MICROPROCESSOR AND C PROGRAMMING (16SMBEPH2)

(Brief notes for reference)

By

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Note: Students are instructed to refer book for study and reference respectively for further elaborate points as prescribed by the University.

UNIT: 1

D COMPONENTS OF DIGITAL COMPUTER. HISTORY:

In 1623, ettre mechanical machines and used for some abothmetic operation.

platse pascal 1642 used a intechantcal adding machine.

Dr 1971 Gattpoled selbelt made an automatic multiplication and devision machine.

Inulte-step machine.

On 1930 19t dégétal computer was

Evolution of digital computer 3

In 1946 ENTAC the digital computer was build.

on 1946 (vonneumann).

GENERATION OF COMPUTERS 3 1stgeneration > 1946-1954 > Electric values IL IBM704 21709 2 UNIVACI => discernbly language Eq : tangible de l'adirectorine e ditencome 2nd generation => 1955-1964 => Toransestor 13 IBM620, OBM7090 > High level larguage £9 3 Nemosul 39rd generation > After 1965 => ICO > IBM 370, 47 peneration → μp. perogeramming. Now-a days for the operation of the system sillicon technology can be replaced by gallium Assenide. Drouges secondary one. the speed of electrons in an It is five times faster, attract ON FIRMMORE ? DIGITAL COMPUTER : 100 MORODER no no digital computer is a programmable machine specially designed for computing purpose . . remains e remained opt Chorge meet · Cart

* A indexe computer ils a small degital computer and a not supply A hardware Brdude electronic , magnetic, mechanical de vices, ord quietation =2 1955-1964 =2 arequistation STOND COMPONENSI & OPDIMER . O DAMAI 21 CPU t pB Memory OF MAR & CORIO devices sign & remaining bies PROBIRAMME = MORE POUSE 94 4 ODAED GO 21 2^{m} A set of sequence of Instruction A set of sugaring task of the to perform a particular task of the 2nv SOFTWARE 3 Software is a set of programme. PERIPHERALS 3016 on and memosey Parts of Input output and memosey 2m it is file almes faster. . alm 2m FIRMWARE S allongueparent program or set of programmes provide en read only memory crom) and other devices prob. piloboga oracion Eg; montron, Editor, Interprotons Change mach to 158).

BLOCK DIAGRAM 3 2m > CPU > OIP 8/P Memory ROMATS BAR cpu of a micro computer its a Note 3micropowcesson » a information its a small digital computer . CPU: CENTRAL PROCESSING UNIT 3-2 -temporary storage Accumulators dec are Greneral purpose) dences compicution Registers and point Brain of niming q the system. ctor units 100mp2C to Performanche i competite's -ALUS Arethmetic Logic Unit. Formal structure of mecocomputer? OPRO. EP ROM/RAM

TYPICAL ORGANISATION ? MP semiconductor T/P memaguy 1.1.2 my che OLP floppy disk und share may consettes computer. TUCAL ! Ra V CPUS CRAMERAL ENANCA Ofference between inforcomputer and micropacesson " Microperocessar ils rone compound of microcomputer ? placemputer ils a complete computer . In interocomputer copil functions are performed by microprocessor. (ma) semiconductor memory 11. Of is the main memory demant of a militacomputer - stated system et used sto

stoke program and data. It istores wooke & RON-Road Only Gemany. Prior permanence Hus comprendenter dereus one pressored as parmony Ot is a non-volatle opermanent Storage . It cannot tobe datas when power is Ot has a dandom access property NIROM Ot contain vassembler, compiler, contents Budgemines venitor, debugging package, other byIO ... nonufadille eraseard permanent programmes: Printer it of its lited for sine, cosine, Manufocusersquare root, log tietc. Prinzeolo 3 users can not write conjung Pacajómed . RON only they can seed. They are simple cheap dense. PROM- Programmable Read Only Memory: Pour - programmable read only tester Menagy. the contents of unprogrammed peak the Base incode up ontheir of 16. The contents of a prop 26 declared by the user. MQ 985 the user can welte permanent pseagerammes en a provo. in each a The programmer uses the prom FROM Lalonencontent is referred to as prom programmer.

EPROM - Estabable programmable Read only semory. at la a 141 the contents are crased by exposing E. PROM to high intensity, short wave wight for site 29, mound the an uv sauce with wowelength of 2537 A whit is used process of changing the content is non-convenient. The writ has to be removed from the boood for exposer do un source, no dians User cannot erase the content of a single memory because entire memory will be exaced. They are cheap sellable and undely used and - marg Electronically Exasable gragoannable EPROM :read only memory => EPROM. they need not be exase from a inforcomputer board for exaring. Mon the charge in the content is mode en melle second. Ch. HIStory

About 10 millisecond is required to write each byte. A single syte of data on entire data can be exased in comilisecond. RAM - Random Access Nemosy: RAM - Random Access memory this mencagy is volbatile. when the paver is twened off dhe context will be destroyed. Two types are available in attais memory. static Rame- (menorus) static Ram, is made up of flipplops. Dynamic Ram! 100 103 28 000 bin Dynamic memosey is modeup of Mos transistor - gotes. It store's like a charge i site inumber of transister gate can de placed on a imemory chip It has high density. Dynamic memory is faster than static memory.

External Organisation :

My As we know, the data is stored. In monogy a cells called with.

Many chips as a total number of N chilts each hauling unique address. (Each bit will have different data.)

The address of whit stanges forom O cho (10-1) abits.

For leading a with the address of whit is referred to the momony.

The memory does the mark by seeading the content of this address and give it on output pin.

Of content le cto de corritten at a particultar address. The chep les supplied with 1) 1 det to de queitten 2) Address at which it is to be written: 3) A signal indicating that a un welle operation on the system to

ube performed. ab tes "Children aganisation has is bit bytes inpuble (fous) acquitaiten. " que pression our r. 8 bet = 1 byte. mon mil sty me NXAbit > Nibble organization. 57199 RAM - TYPICAL CONFIGURATION + CORDER saturd and wanted strangets. addinger 1 20003 5 Jodata 11 Read 22000 OT 6 CONDITION DESABLE write 3300 ours 3 bootond. Power supply chip and a dista of charging : (3 disable. A list will be the other control 2/13, 0/5 enable auxite operation . co then a cond crond from alle implete * All memory chips will have pens on which address of the bit to be read ar mrite de to be supplied. * According to memory size, the number of plas are available. Egt in a 2K byte memory it has 11 address input (105) (10 to 10)

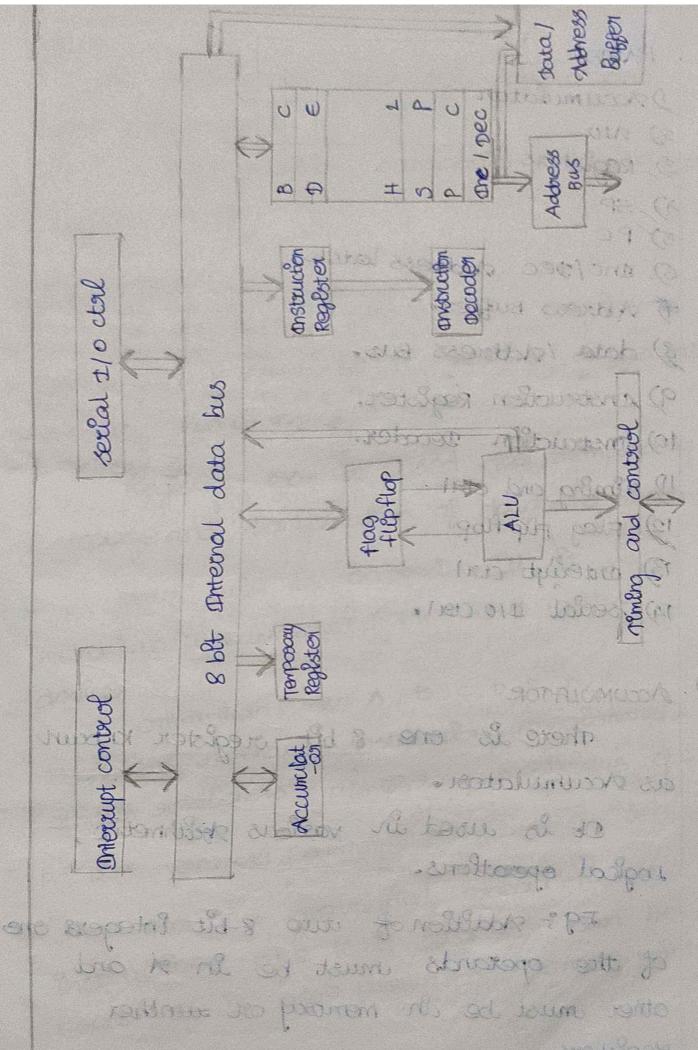
No lo 15B Here, Shio Is MOB * FOA a larger chip (16K), the oddress are split into some duistins. The oddress Input plus is under address multiplering. Read and welte inputs: On some chips there is only one Input to Indicate the read or write operation instead of two inputs. Eg: 2142 RAM. In this model WE is a single pin which with read and wilte operation. co Fast stead operation the Popul is high For worker operation the Brout is how it is a second at the contraction is chilp enable on desable 3 min to min. Before any operation stre chip must ube in active grasition and hence, it is initially enabled by actiliating the input. STOTE I BEA

However, for an EPROM OF PROM data is input at the pins. As these are as the output which are provided Fasi data input to the chip of waite operation and abta cutput from the chip con acad operation. Improve proof in output desable input ? Sites rough it Thus is provided on many chips to inendeling the data stead from the memory on its the data pens. also delected before data can be priss i dead prom the output pensionality (1) Power supply anped? Supply as denoted by vcc. Nostly It is Svolt we maple other control Input / output signal? work i) Address Latching In some chips input is provided at the failing (091) statisting edge.

of which the chip latches the address available on its address pin. rêg c After the address has been latched Inside the chip the external address Inside the chip the external address on address pins is no mosile used. I Ready Output + After the chip selection this goes loward size input is cactive. the * of it goes high at ealing edge of the next cycle, this cutput clan be used by some micropsiocessosis to pertend the specer delecting stree also delet deleged dele service della servic on chips requising address multiplexing sustable inputs one provided in most using these inputs the chip is informed if iss on MSB of the pobless thave obeen placed in odbitess pin. entreer construct conput l'autrus à an come chips apput les provided 3) subsess farching + sta balling (cir) science edge.

Nacaopaocesson Architecture: UNIT-2 8085 is an <u>Bibit</u> microprocessor. available as a 40 pin - dual inline Package . The data bus is 8-bit wide which imples that 8 with of data coan be transferred to ar from 8085 processor porallely. There are <u>spins</u> which are detlcated to transmitt 8MSB blts of memory oddress. This where The 19B of 8 ubit of address are retracted on the 8 lines on which data its transmitted. Thus, the data and apart of the address are transmitted over a set of shared lines. This is known as <u>multiplexing</u>. Hence, 8085 that 16 bit address -tocanomission capability.

A los apprendentes a secondance and the second day and a second coujotal AB-MIS (Address BUG in Sector data and piled of the tooler with control , pro l'arrangements. social data or 00/5 · Part marin 216 Momosy locations can be attressed Application of causimat by 8085 . Each location is a 8-bet of data is transferred in parallel between the 8085 and the memory. 60, 8085 can address for 64 KB of meniosy. and apoint & the contracts are transmitted where a net of allowed . Brees this is N BOUNT OD ANULLINGERING 1 HORE, SUBS HAR IS DIE OLDEST - violation . Manufacture -



PARTSA DAccumulator 1 2) \$10 3) Registers a son ± 63 00 A), SP 5YPC 6), Oncidec address latch Address Buggert. > is rocated in and suf and Ad data ges to commul with cpu - The normany a Ilo chips comeded to 8) data / Address Bus . these buses the cru cou escharge desired data with mence 1/ochips. 9) Onstruction Register, > 8-bit 2 g. when off instru is detched growing than it 10) Distruction Decoder stored in postruc regis . Distru 1) Thinking and etal = decoder detades the finto present 12 Flag Flipflop 13) Onterryt ctal 14) sectal \$10 ctal: -> It ctals social data commu by Using these 2 institutes stocked sol. 1) ACCUMULATOR There is one 8 bit register known as Accumulator. at is connected to internal data bus and ALU It is used in various speathmetic, Logical operations. I/o \$ Load 1 store opportions. Eg : Addltion of itwo 8-bit integers one of the operands must be in x and other must be in memory or mather registers.

All delthurtetic and logic operations are performed. ALU Egg Addlition, subsidetion', logical AND, e Dankitste logical or etc. NON RIGIOTERS !!! No me provo, the various regleters A, B, C, D, E, H, L) SP. PC having different mencery locations. Jach-Hold &-bit data Register ican be used foor temporary storage and wantperlation of data and Instruction. Data well be staded till It. Is send to the memory an input routput are is used its se devices. then, the A, B, C, D, E, H, L other than, the A, B, C, D, E, H, L Registers we have instruction , registors, status registers, temporary registors etc. PC => Psiagramme courter. (?) () 1000 (? For the sequential execution of instructions the 16 bit register oan be used. It is also known as memory pointer.

The function of programme counter & to point the memory address from annungen the next byte is to be fetched, When 8-bit is being fetched. The Psuggiamme counter lo incremented by one point to the rest location. No Sop's stack pointer anscielses 16-bit At is used by the programmer raid Bretzynton. 21FO do malhtain is used by i a stade In the memory, of holds the address of stack stop? is preaments the content of a acgister during execution. Other with the stack which is always It /- 45450 during Elag Register put & pop openations top it Elag Register many statistics i) covoy (E)(CS) At is an 8-bit aregister ii) zero (Z) having Alventabits früp flaps iii) zero (Z) having Alventabits früp flaps iii) sign (S) of the holds either 0 on 1 iii) sign (S) of the holds either 0 on 1 iii) partity (CP) the di gather arequirestator. iii) partity (CP) the di gather arequirestator. monthay possible will any carry one of the books

Deavey - This status flag holds coury out of the MSB resulting from the execution of an arithmetic operations. If there is a cavery from addition On subtraction (bourse) on compariston the (s flog is set to me otherwise zero. Lovi) a zero status flag is set to one. If the desult of ailthmetic on logical operation is zero. Eg: 11 Fog non-zero gresuit it is zero. It's data true in 8-134 while . 60 II) sign (5) The sign status flog is set to one. of the MSB of the result of an arclithmetic ar logical operation is one otherwise Zero. Poparity (P) PO) paveity (P) This is set to one when the desult of the operation contains even (erA-8A) Syd. runber of ones and it is zero when It is odd onumber of ones particulation (A201-1923)

Auxillary carry (nc) store date proof This kolds cavery out of bit 3-4 resulting from the execution of an avertametic operation. isted to teled at dialated read (EV. B) A ZERT LEOTUR TON A 200 LOT LOOME Joséphie and pits were and ge Data bus - Address bus 0992 a roltogang and the the Intel 8085 is a 8-bet 12lapsucesson. of the data bus is 8-bite unde so, 8-bit of data can be transmitted in Parallel from (69) to the incoprocessor. Intel 8085 requires a 16-bit cuide odducess bus as othe memory addicesses ave of 16-bit Por poor set (P) The 8 MSB of the addresses are event transmitted by the address bis (A8-A15). a character of The BISB of oddresses are itsansmitted by the oddress or data bus. (ADO - ADA)

The data and address are transmitted at different moment by abbus. At a porticulari alme il transmitts data or address (time shared mode). This is called multiplexing is a con partition 16-bit is initially ctransmitted by Then, 819B & address is latched. mergeacessog with a with 190 that, complete 16-bit addresses remains available for further operation. Now, 8-bit 10 bus becomes free and wilt is available for data trans--mession. . ships hughts 288091. Pin Configuration of 8085 (1111) 131/0 (1 24 ton Vgnd ADO-ADI VCC in endlied A8-ALS RESET IN -STORE SORE SCIKON RESETANT < - HOLD She Alanog atris HLDAD TIO M 30 51 TRAP AIS). RST 7,5 RD 2 WR -RST 6.5 ALE CATES SUITED D RST 55 SID ENTR SID - SID - THA READY ->

3-4

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pultiplezed address. Address, databus D) <u>AR-A155 (OPPPON</u> <u>These are the address his and</u> A) IO/M COIPS 3) ALE" (centriput) Ot goes fligh when first clock GIT + TW - OCK (2) advers (co) [I/0] address during first click apple of mentiony eyde. They are used for data during second and The use white of the address the be the set is a status signal theman latched into perspherals around address worth places in the side used for the MSB of the monuscry address (co) 8-bits of Input located third cycle. menuant 20 arres & 20 road poor distinguishes differentiates. of the angendant correst VEAG J WR (OIP) 5) SOISI COIPI 6) RD COIP Signal to control seed operation #) WR (OIP) Signal so central wette peration. " Signal so central wette peration. " en proper de la properte la properte de shout. The data on the line is loaded that the bet of the accumulation. Enough when kin instandion is executed. to see si so operadient 1 - So operadient 1 - Petch 1 - Petch when It is lever) the address on the address hus & for senary. attress is for mentiony (on) I/0. address bus is for I to devices. when It is 1 the advess on the

12) HOLD (TEIP) TRES Implies that another master is sequesting the use of so Bus having (alla) (alla) 10) READY CIP ID CLK COIPS velinsulates the use of the buses, as accelled a How sequest the introprocesson It is used by microprocessar to sense if the phecipherals is ready. Is some at which the processor geodes. the #14, of accumulation is outputed. used for other digital Ic's. It's frequery READY is a then the independentian has do deansfer data (cer) not: CLK œutput for user. This wan be at is a data line for sevial of seensy is 1 perceptional is ready. If S BOBICON Signal for HoLD acknowledgement. These biteringts when at biteringt RST 7.5, 6.5 and 6.5 are the sestant RST 5.5, RST 65, RST 7.5 This has the highest periodity among interaupts. This at is a mon-maskable TROP (STP) Intervenpt. Fact of their has a programmable completed. HIDV (016) de automotic one. seen as the worlent machine cycle is HOLD elemented. The processon regains the bus often they cause an Interrupt destant to after HOLD is aremoved that is zero.

disabled by softwares. An interrupt lissue and to you The INTR line is sampled in the last state of last machine cycle of TWIR CEIP) indropenesson without the wastage of the. by the deulice to transfer data to the INTA signal. The IMP is enabled or an instruction. In error 1 the production accordingledges the Intercrupt signal and lesues an the introprocession supports, it havenal sequence of instrumbions. After completing the Instruction at hand It goes to call Inspection. the above preliciely shows the lavest Increment Its content. at is unaglected by any mask. At is an interrupt signal. So, 24 Constrain mlingpacement after the INTE & secreted. TIMING AND CONTROL UNIT + Valor prosention and execution 25 the dealtrailet during a certain time sut Each of these fetch and execute are performed in time slot of forced (on ranging length?) power is the two tasks are sequential A the state of fored with whereas, further step. The two tasks & fetching and me two tasks & fetching and executing instructions are seperaturely executed by the microprocesson will loop for beginning the fetch operation the nect. INTA COLD stablizes. The inderopsicesson enters a interrupt acknealed prient sent by the while power is on the input voltage

may be mare than I byte long contraining data or gerand address. real for redging the <u>Et C</u> of norther without the test of the rest of the test of tes byte containing the operation code can be therapping to information code indersperchesser keeps stack of etherical adviness of ether next instruction to the exercised and the etherical the etherical and the etherical and the etherical the etherical and the etherical and the etherical the etherical and the etherical and the etherical and the etherical the etherical and the etherical and the etherical and the etherical and the etherical the etherical and the ether to be executed, therefore, Instruction cycle, to applicat to feth cycle + execute cycle. time slots out the length deling dependent on the instruction the sc operation sequine variable might Form the memory the Distenction sand ac - obeloner the section of the se and the addressing made specifies Appresance Norde 3. 200 year after decoding and execute operation are general purpose suggisters. Then, only ubyte long the operands one in the the address field of the Instruction. a sure for Britespretling (On) malifying cycle depends on the instruction type. the operand is actually referred. Because, i it is no be done before acconnotating one as both of the provisions performed resources sites subscript, (*) of the Instantion to only a rechnique for the purpose of The stime acquired for an execute systems used addressing mode

Dommediate mode. Egg CMA > COMPLEMENT ACCUMULATOR. degrillion of the Instruction. J' Amplied mode. THUBLED MODEL & PLAT WORKDON ONTO alle generic and one one harding are specified implicitly in the Its particular addressing mode. address fleld may be associated with than one address field and each FORMAT! " The state of the state state state . In stubs Pinplied made, the operands BASIC OPERATIONS OF THE CYCLE ? 9) Fetch the Instruction from the 3) Execute the Instruction. (2) secode the Instruction is not for (1) An instruction may have more the the states opcade made address There are two modes ? o anno 200 (2) democratic ANG colores ! 40 12 in The particular register is selected the cpu success O REALISTER MODE :- 1010 uner the address field specifies are in register that reside within IMMEDIATE HODE ? made Instructions. Egs cmpr > compare Reglater form a suggister fled in the instruction. Is sold to be 'In the register mode With grownulated. en a procession subject. advess field. may specify either a memory mored a processor register. The instruction stat use an accumulation are implied has an operand fled auther than an All registers référence instruction An inmediate made instruction The address fled of an Instruction In this suggister mode, the operands interfect of the set con the anness the closest wand NOV -ADD

mades it is essential to sufferentiate address is specified for an operand indirectly). the accumulation in the first instruction son de positiculars seglister which has a positicular, oddress donaidering a table 0 Eg & 10A 2020 Joodo & alloted to the addiess part & the Instruction Scientifical. The data can be stored after the address the operand can be and the effective address piecel by of data in monorer [. monom ni atro go memory address & the operand lest stegister Indirect model Instruction the address of the openand exather thank REGISTER ANDIRECT MODE : the operand starts. Before using a placed in the processon register, with the a previous Instruction. Propammer unust ensure that the All dedores and acore manually The selected elegister contains the control when executing the herrich (COA) The who we have the fall of DIRECT ADDRESSING NODE :computational alctated by the gliph addressing the Instruction. memory , control. fetches, Instruction the effective address is stopled in the umade. TWDIRECT ADDRESSINGI MODE 3given derectly by the address field of is in memory and its address is memory address abtorned to gram the from memory and uses sto address Instruction gives the address . where, part of the Instruction. The operand address is equal to the address FATECTIVE, ANDRESS 3 the effective address. part to access memory again to seal effective address 25 defined as the In direct address mode, the effective Here, the oddress fletd of the Egs STA 16 Left -> store to accumulation 10~ 16 bit

Delt. INDIRECT when compared to the direct type. mode, the memory spends more bits and the service of th Reparing to the Indirect addressing easy setting nodes since contracts for in the transfer and NOO - 40-50-50 easu NODE Agreep another 0 mindage and and a EVERYTHINE COUNCIL Carter Poro Internitione Cricke. 200 Contrario anapulare to excess mention Empleed sources we 35 Erevels righton gress the 22 elanar 1. Puperand. the entries JUNE DAVE P.D.M. ICPAC Direction . 1350 LOL PADD 6996d 2157 adruct 3 350 -DEC - Unorte --14200 A RANK Parent Cat JUNK Acountibutal the number of usits sequined for the a smaller number of upers. compared, to gletative address can be specified with in the instruction format. since, the of the next Instruction. constants memory is relative to the address algred number (two's complement)." memory address , and a tart content of PC stre scesult produces an the content of the programme counter effective address unase position in obtain the effective address. Is added to address part involves to Since, the should address field megative-usits to best when this number is added to an this relative addressing made, RELATIVE ADDRESSING MODE : The address post is usually a which can be efficient possible a actions she the redunded encourse Streeners the ratio burtigeout to

to indirect attress mode. an this indered addressing mode the address field & instruction define the beginning address & data avoid if monory. tack opened is deter beginning address and the operand address Instruction is obtain the effective address. INDEXED ADDRESS ING MODE so athe Indoned beginning address , that contain a linder and the inder value the content of an underted ineglister la provision to increment the address field. addred to the address part of the related to the beginning address. chi register that contains an englister The Indexed addressing made have a The Indexed Register is special ruper cf. In this base register addressing In the way that they are used sather than they are computed. to obtain a effective address. unde the difference, between two mode is added up the address part of the Instruction BASE REGISTER ADDRESSING MODE ? updating to the new segment. in computers to facilitate the selocation the Instaulton. Alls register is used only the value of the babe register requires Programme in inemident. work to the hold a wase advess and advess fled of node the content of a base stepleter is from the segment to other. the, address value of Instruction do not have to dange change of possiblem ... value of Instruction must suffect thes unken data at programmes change The's is similar to the indered register This wase separater is assumed to with a base sequences the disponent 100 m m

a sig is the second sequence . For For mov set se as a copied from (1) Nove INSTRUCTIONS? at also transfer an Immediate date se register ex mensory. Here, ad 25, the register that menory to register. or copy a data from register to acts as a source designation and regester on regester to memory on DATA TRANSFER INSTRUCTIONS - (2) & movies Register & to register By a plinting. sate transfer Instruction transfer IGN NOW SBT A 6 pm register prior Farman & LX2 9p, data 16 Bg & LX2 H, 2000 10, 10, 4 FORMATS MUT SI, data 8 MAT SI datas Here, <u>r</u> is a general prespose Register (1, byte) Eg = nor 10 . A prespose * Load simmediate Register pair = This Snotewation is used to load The letter in is used to represent a 6 bit immediate data into a specifical locations and each has distinct address. * Nove annellate Instructions 3 Memory, there are thousand & memory the to a style instruction . * nove between Regisser and memory

This instruction stores the contert Shaples the contents of the Accumulation in the memory unionse address ha memory location whose address is accumulators with a byte from the that changed . address in 2550, which is a de alter of the occumulator on the memory whatse specked & the Enstruction Stoelf . * Shore Accumulated Direct Before The content of the decumulation is South And The Party Lood Accumulation direct loads the Eq. STA 2550 (1) 1 1 / Ling phase A Association and A 1.C.A ARITHMETIC TWSTRUCTIONS apages approximates and to the to a specified register on memory to the contents of the same uptor. a) dans willer and herder in the weeks memory location to another . proton whose address site the subbocken, whit snowment, descement are used to perform addition, to transfer data delectly from one * The artitumetic group of instructions No Instruction & available in 2085. Mon m are used to the contents the prop Enstauctions ADD is and specified in the Intrauction Rescile. Eq ; JOA 2450 This copies the contents of the memory Thils in a three byte " instruction. Martin States Contra the stand when the

flags. is used to the contents of a t the accumulation of stamping and the with carry flag to the contents of Enduded in the instruction steels. d) ADD Immediates with coury 5 miles (0 specified register (on memory along m) ADD with carry instruction this instruction is of the fam contents of the occumulation with an showing deal 8-bit data, les enduded. Subtras aires All uppes of ADD Instructions affects accumulation with an <u>a bit</u> data. (e) SACATOR - 2 (nalded adds the content of the are may to the 200 36 consist ACT data 8. This add with carey. The b) And innaliate The AND Immediate instruction ofter a solar at an ather ADC W- HER MOSTORIUS

H TOTAL SA flags. with covery glag to the contents of is used to pop the contents of a the accumulation of ustantitude anti- x-(12) data adds the content of the Enduded in the instruction steely . d) ADD Somediate with carry 5 and 10 specified register (On memory along " c) ADD with carry instruction accumulation with an <u>8 bits</u> data. (e) these instruction is of the form contents of the accumulation with an 8-blt data, les Enduded. attrations arts And Mar Mar 1020 all NOI data 8. This add with casey. The b) And immediate The AD Immediate instruction All uppes of ADD Instructions affects c) sub with boxed - war and d) sub momediate with barrows in C a) sub with register on memory. with boscow flog to the contents of a specified suggester (an) memory along is used to subhad the contents of the Enstruction Stells . 1917 with an 8 ult data. Res induded or SUB Sommediate : the damulaton. SBI data 8. the centents of the accumulation + of a specified sneghter on memory to subtact the contents of the accumulator SUB more used to the contents Subradlen & The SUB mmediate Instruction (SBI data 8) the sub instanctions sub and the instauction is fithe form The sub with barrow Prsteucton Eq 5 SBB at the training 1 1 SBB N y or design these

\$ Increment segent increments of Increment segent increments by Increment segent increments and the segent increments A sequent suggester passi-by I with steppet to & c, they H is and by I with steppet to & c, they H is and by I with steppet to a sec they H is and by I with steppet to a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is and by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with steppet to be a sec they H is a sec by I with stepped to be a sec they H is a sec by I with stepped to be a sec they H is a sec by I with stepped to be a sec they H is a sec by I with stepped to be a sec they H is a sec by I with stepped to be a sec they H is a sec by I with stepped to be a sec they H is a sec t content & the segleter by 1. Eg & Inx apple scaland are (h the accumulater with an 8-bit data This sub with boscow. The contents of pe) sheudod. All types of SUB Instructions offer The Instruction increments the 、此 ひまた 阿田の A) pouble AND meterudion ? @ recomment register polisist content of the reglister by 1. of the specified neglister pairs to the O Decement register / menury + align the second state and the second s Decrement : Automatic Antio This Instruction decrements the This sustances apply the contents gf JCR M JCR B JCR B CIE bits Egg ICX UTP by 1 wood, to Bes DES HI and SP A suggister paths used to decrement Eg & DAD SIP . 1 Log < Log 1 - 1 - 1 - 1 - Co

The ANA'SI whis Instruction performs B) AND IMPOSIBILITY IN INCLUSION AND INCOMPANY AND INCOMPA accumulator and the immediate data. operations with the contents & the most for butowing vogens rober This Enstruction performs logical AND operation between the contents of the specified sugister and scennulater ugical AND operation between the a) and with regilenter / memory ; thog is set. In and we at modifies the plags s, z and p LOGICAL INSTRUCTIONS & THE ST cy flag is always subject and ha rogic instructions in 8085 are B OR ANOTROCTIONS & Here, ANA et and be used for masking specific bitrs. operation between the contents of the under is given in the instruction lisely. b) OR INMEDIATE S CUUSING CUUSING cy plag is always select and ac plag is set. It malifies the flag six and P. JORA M DIE STATE cy flog is always specet and she flog is set. a) OR INITH REGIBTER (MEMORY : specified register and documulator. logical or operation between the Here, ANA or and ANIT data 8, can at modifies the flogs sit and P The of device the war of the This instruction performs logical or The ORA & this instruction performe ORI data 8. 100 cm (1.5)

To long a the top of a solution and chercitar promises and culture of ad W CR WHY SCHUDNALISNE NO -X3 (W cy plag is always resolved at inder a chear le that many and a the used for marking specific lits. which is given in the instruction accumulators and annealiate data specified register and accumulator. a) EX-OR WITH REGISTER I MEMORY the xpp of Instaudion pologins It modifies the flag sizard prological ex-or operation between the AC flog la set. look of the y flag la always neset and at modifies the glag Sizand P the gratemator perfor due or u used for masking specific tits. a) compare mith register (memosy ? flog is set almost nonunitary with Here, NRA 31 and XRI datas can be accumulator and ammediate data. operation seturen the contents of the this Instruction performs legical exor Comport in which is gluen in the Instruction at modifies the flog on S, z and P. cy flag is always sneset and sc stockf . of the seglister I memory with that These instructions comports the contents of the accumulator. Jon XRI data 8 mention The comparison is performed by Cmp m

) ROTATE ACCUMULATOR LEFT WITHOUT OARRY - CRUS the Instantion RLC adates one let possion to be left. specified registrans/ viennary from the contents of the acclimation why ROTATE INSTRUCTION 5 that of the accumulator. subtracting the contents of the is a content by subbraction . une contempor to teleanor of Immediate byte with the occumulation not charged after the execution of This instruction compare the b) COMPARE EMMEDIATE & Here, SIP, Ac flags are modified. (h) contract a warm ration) Erect a The MSB bit D+ is shifted to the 14K to the con flag stet and madified. ISB Do 1 1 0 1 0 1 1 1 V also, the DT but comes the coury After executing RLC Enstruction D7 Accumentation D7 76 05 24 D3 D2 D1 D0 MSB 1 1 1 1 0 1 0 0 CIDOIOIII) 1 00 1 LSB

is ROTATE ACCUMULATOR LEFT THROUGH HI CARRY! AF CY Alice exerting IT. OC. The BST The accumulator by one bit position to te left trangh carry. too eqi qt 5 2 The MB bit of ls shipted to the 10K After Executing RAL Alwargh covery. The PAL Rotates the contents of 0 +1 0 0 1 0 1 1 1 1 27 J2 25 24 23 02 D1 20 MBB 1 1 0 1 10 27 26 35 By nutation 2 21 Do 0 13 ") ROMME ACCOMULATOR RIGHT WORHOUT CARRY !course flog but and unodified. position to be slight . of the occumulation by one able Foor eq; 97 To]the 158 wet 20. After executing RRC The RRC redates the contentes The MSB bit of la shifted to Also, the DI Jolt cames the - Angel MSB the second second second 0/1/0/0 1 9 1 0 9 Steel House LSB 00

i) ROTATE ACUMULATOR RIGHT THROUGH 1 10 1001011 coard. CAREY the accumulation by one usit position to 198 195 20 be adopt with warry. Foa eg: 94 14 The BAR states the contents of cy The MSB DT is shipled to the spear executives BAR thocaugh 1 × N55 97 The to be set the 40 1 10 100 00 00 0, 90 JSB --> DO · KOGUL instanction : Special anotavotions: oddition is performed. connect BCD . everyult . when BCD (54A)

net offected. In the occumulation. Here, flags are gesult only after an addition or is used to produce 800 securit flag. Internally and not available for the only for the data in the accumulation. inconent operation which affect the to get the connect BCD prosult. It ONA is used to peraturce BCD () Complement shacomolynor : The anallowy worth 25 west and Instruction is applicable the CMP complements each bit

1) pedinal adjust accumulation o estipoid an part of 400

1) LOAD ACCOMULATION AND RECT?) STORE ACCUMULATOR INDIRECT ? content of the accumulation in a JEJ pron'EN - a annutant memory location whose address is content of the accumulatoes in a The stax B segments int The Shatsuction STAX B stores the course glog do 1 The Instruction LDAX B Lood the W COMPLEMENT CARRY: ili) ser CARRY: The Instauction STC sets the the covery flog DATA TRANSFER ANOTRUCTION - 2 No flags are affected. The Bridgeudtan (inc complements Eq. STAX D Manager 3 () TY LOAD HAND & DIRECT ! LUN I ID STORE H WWD I DIRECT : load the content of 1H specificter and c segretor. In two successive memory pocations. I have a few seconds 1 javer oddress and the contents of the to moved to a memory having a high segister. His moved to a memory maked to a memory have a successive memory pocations Argh suggister and uses. deglister and I deglister in two used to stone the content of H memory location whose address is Chadar +17 CH2 +1 12 The convents of low register 1 is The Instruction SHID Address its The LHLD Address is used to egt 10AX D allow a structure at a

a sette so be seed or surfitten indo. In This instruction Exchanges the contents of HI pair with se pair . [4 1] くう [36] the mean time the people center is vi) copy Hard L RESILETERS to the V) EXCHANCE THE REQUETER PAIR HL and Se the address of the memory location. For register + is moved to a memory toring STACK POLNTER: a higher address. haven address and the contents of high BRANCH INSTRUCTION ' se the Instaution XCHGI stack polyter . contents of Hard L Registers Brite the stack pointer. This formution SPHL Loads the していたいという 8085 youngaam counter sends out (Addent) <- (H) automatically incremented and is ready

ex: Jmp 2550 j jorap INSTRUCTION[™]
 ⇒ uncarditional sump
 ⇒ corditional sump It is store. Thus is a 3 byte insteadon with the commoniant Jump . The conditional Jump Instauctions such as. with the oddiess of the next memory location of the year Jimp address 16 - . UNCONDITIONAL JUMP Sup Jub Jub Jub 1 controlling the oddress. first syte containing the opcode Conadure ooder of the Instantion and abyte 2 and 3 The utconditional jump instruction is Juz - Jump 28 o glag 28 not set. Jz - Jump ils offer les set.

The graup of Instruction which are to the propertiest work the stand by a separate memory black. This block is genup called subscattion to the frame (C) (C) and a super programment of any a correst i under Jerarch Instruction . Florst we should inter - inter 20 a feel to inter where that the substitutes are different moth program the subrathe to called. space is rando. This bidgen is solved in a elegant may. Jc - Jump 28 Landy Blag bolder with JNC - Jump B carry flag lo not set ab - Jump SB slgn flag sen not roct. CALL AND RETIDEN ANOTRUGIEN ACTUL STOR IN JPO - Jump le partity flag his not set , -SPE - Jump - By Janling flag - Es get 11 JM - Jump unen "skin flag is set. To wall and even instruction and C RNZ - Return if zero flog is not al. has to settles to the main program. At the end of the subscutture, the participations These are proportion are allocate and satur Now the precederate to prevente the CONDITIONAL CALL ANSTRUCTIONS SUCH AS+ RE-Return if warry bag is set CONDITIONAL RETURD ANOTRUCTION GUCH AS : RNG, - Return if would flag is not ad. RPE - Return if yould flag is not ad. RPO - Return if partity flag is not at. RZ - Return 28 zero flog is set . The purish badd, upper the main man set. en apo - call if pailey flog is not set j) unconditional call and stemmer. Mul is conditional scale and settion of on - wall when sligh flog its act. and - call if warey flag is not set. ope- wall if parily that la set. a - call le carry plag is set. CNZ - wall if zero flag is not set. cz- call if zero flog is set. EX.3 CALL 2550 CALL ordiness 16

icontent of a sieglisters has to be saved acquer in the other part & program. for future use . sofare using the same . A omail area of the read or the sea of the states of the second at the Stook . matter monioned know can be coalled as STACK AND STACK, RELATED SUBTRUCTIONS : ate way is training thirds the set suggisters what have to use again and ogain. The byte instructions in his difference is Ron testum if sligh glag its set a most the real a man b least the ep- Return if sign flag is not set. The A RET 4 the ALREN 2 and the start all on all use the propern, the an - roll mark with head an Restart structured are opecial one in m There are g septert instruction. CAREFICE CALL CONTROL OF THE LAND TO AND Rgr 6 1000 gi uno vo Port o AL DE 2012 1040 × 20 PUSH & pushes the data on content Is used and to setable the data or The push instruction is used to content pop braceleten is used. To save the sugesion push instruction the contents of so pale is saved in conce and the contents of a register of BC regester on the stack the burges NSH as stoke a neglister whe pair The pop instruction its used to transfer POP : the stack and the value is determined. Is stated in the memory (sp-1). ar stack . two bytes from the top of the short to erecuted . the sequence in specified. NUMBER OF STREET STREET STREET STREET The stack politer is idectionented New, If the Instruction push & is Eg + push B . Courts uniter of The Britter of The

MACHINE INSTRUCTION / MACHINE CONTROL ANSTRUCTION 1 accumulation of a set of the set a type from an eutput part to the 125 the out instruction is used to output fram an input port to the accumulation the en instruction is to input a lyre To another tous : To communicate with the entries and moved the processor uses that ports and super price of satisfies and the sequeters are said and serviced SUT De cettor en consistente, avec d'a una d'a una de ancientes de ancient M TO AND MACHINE INSTRUCTIONS : on a last In flust out basis (uro). + INGLEUCTIONS: de commense sins sous sous rushed in last must be reprod out firsts this means the predister pain that is of account who are memory and the ser.

and no further instructions are executed. I) HALT INOTRUCTION : The HIT butenchen stops the nucroprocessed

UNIT-03

8-bit addition

PROGIRAM ;

10A 2050H ; take the flast number A

NOV BIA ; transfer the number

from a Into B.

10A 2051H : Take the second number

K B

ALGORITHM: accumulator . in coccumulator in the memory location accumulation the menuary pocation 20514 to the 2052H the memory location 2050H to the B requister. STEP :6 ENDstep:5 store the result which is STEP: 1 Get the first number from snep:4 add the number in A and B step:3 Get the second number farm step:2 save the first number in

2052° of

outhout

INPUT data 2050:03

2051:04

1

mode instructions like nov sim and

MON MIA are used .

STEP 2° Register indirect addressling

menually location 205241 MATHEREN

added and the snesult is to the

memory locations (3050H and 2051 H are

STEP 13 The numbers shared at

HIT ; and of peropoun.

memory

STA 2052H ; stage the sesult by

ADD . & ; add the two number on

2050H with THI register.

STEP 1: Initialize the memory location

ALGORITHIN 9

Example 3-

a) 8-ble addition with cavey caccumulator. the monory location 2051 H to the step 2: Get the filet number facant the memory lacation 2000 to the siegisten steps: Get the second number from step 7 ; end , the content of the memory location memory location 2050H. In the accumulation 2059H STEPS: movement the address by one. STEPH: and the numbers in t and steps: ancient the oddress by one. accumulater A. occumulater in the memory location STEP 6: shore the sesut which is bu ALGIORIAHW ? New the address is 2052H. The memory address ls 2051+1 STEP2: some the forst number on B Step1 : But the first number for the the state was the subdurban prevention as STA 2052H ; shore the result or NVI CLOCH ; clease the second. Jump to the locatter PROGRAM STUDIES , SHOLL) MOUTHINGS caucol & E siegleten. step 8 : store the carry in memory. step 9 : end. ADD BOOS and the two numbers · chunder induction of the chunder stept: store the result in memory. carcel . Jourderand and Andrew Connection SEPT: LON 2050H; take the forst step 6: The eavey produced which is steps: add the number in dard B STEPH: clear the c register to stope DR, C ; Else, Incoment c register is the constrain FFM, in INC GOTO Mov B.A 's manufer the forst unamed Goro. ; of the susult is less

mennoay.

in and the stability . HUT ; End of yacopann. the total date on second 32 bit on out bit "descriptions, my changing president want be that he feetparts depend runter and balladical with prepuber two mencery location . The the mental of the place of aller act of these two plus intropic atime remations which of 16 likes . mumbers are added - Let us take 64-blt stellation)? Example 1 anjor data 2050: 89 (adderd) : percebant amp i unadorida Really 2052 : HC CARRY + 2053 : 01 actives of the forst number of makets to also would bu ADDITION (16-182 32 the and 2051 : C3 (gugend) THE A DUTY

alipeara soss : 32 MONTH (3) 62H - HUH - 3CH a uliger sumber distalled a guilible The ... conver to Hors. subtracted the analter transfer from and a contract of DANDE . SUB B 3 Note: PROGRAM 5 Sin 2002H 3 shale the difference in A STATE AND A STATE AND A mat : : : : : : : : : NOV BIR ION 2001H : Make the second number annut data 2000 : 49 (countractul)on se counde glion une sous LOA 20504 ; Take the ford number and the anonexy countered in A 2051 195 (Munad) a contract of the second of i subtract the flort. ; Talander the stimuter othe second number. opumber from. (minuerd) in A.

Hur the good of uperception. address of the first number of and a company and the second of the second of the first dation second. tumbers are added tet us take two numbers are added to bets. oraquise two memory locations. The 32-bit, as at - bit identitions, by changing the immonity in the place of elther second number are initialized with property can be used to perform Hi and to be to stagistict . 0100 CAREY > 2053 : 01 Each of these two byte numbers 64-bit addition 3 10 10 10 1 INJUT data 2050: 89 (Adderd) : result to also showed by Appirtion (16-bet) 32-bet and 2051 : C3 (Augend) paragram, due multilité

The country to Hord. Processors: marce the fort number country i marce the fort number where bin i reproduct the fort number where bin i reproduct the fort where is i amonaged the fort where: and the conduct the fort and the conduct only form and the conduct only

3) 8-BIT SUBTRACTION WITH BORROW? ! STEP 4 STEP3: Get the second number (milliond) Steps: stone the first number on to ALGORITHM'S when a sloper number is subtracted Jacon. a smaller number. munder, me mill get a megative Poreguan , A posicie (carry flag) occurs will be shared in a's complement STEP1 : Get the first runner (subtrained) the next pourpounts we get the differ-Indicated by setting woorry flog. an this case a occurs which is spault. les cardin the negative meauth the higher number from the smaller ent as well as the based . from in the memory as the on : where a stepfisher to store the Martin Antonia It is similar to odd with covery Jorom the memory to the accumu-Strom the memory to the accumulat lamer " on the other hand, of me sublight SUCTION (1) 200 step 95 End. STEP 8: share the boucew in memory PROGRAM 3 10 1 1 step # : store the difference an stop 6: af the fight number & bigger JNC GIOTO sneps " subhact the subhaerd form sub B 1 subtract the subtract 101 2051 H & Take the included & A ENR C. boarder, if the 1st number is bloger MUT CLOOH y clean the c regester. than the second. than the second volumbers on 10A 2050H ; Take the subbaond Bry nov bin i mansfer the subboend the monuerd. saued in c siegester. borrier is produced withith is momosey. i of these is no board ; shore the bornau Puto B A CONTRACT & SOUTH pregester to In named Guoto Else, "Indement a" Jump to the location

ALGIORITHM ? step :3 bet the alkalend forom the step: 5 and emerd the c neglecter. STEPH philiplice the congister -laton. STA 2053H ; shalle the booker in step : 2 save the division is B register. memory location 2050H to the accumulate memory location 2051H to the occumu STEP 37 get the division from the Example ! HLT ; End of priogram. STA 2050H ; shore the difference bu nov suc ; more the bostom on a Inputable : 2050 :04 - anemory BORROW : 2053 : 01 RESULT : 2052 :01 menrosul-2051:03 the fort memory. Step; 10. store the gutlent is non-out steps of stone the standad bu and & to get the remainder. step: ? If the didend is less than step it the the dividerd is quarter the divisor, and the contents of A step: 11 end. the division, then go to steps. steps subtact the dilloa from PROGRAMI HERE INR, c; Indement c register MVI C, FFA : Initialize c register 20A 2051H : take the dividend NOV BIR ; reansfer the divisor 12A 2000H; take the divisor to to b register. to accumulation. content by one.

White dissingenainder. greater than the divisory then go to the location. named HERE. RESULT 10 2052 : 03 STA 2052H i stople the quotient from the devederal. Example' saladit MOV AC STA 2053 H SUB B - subtract the devision. JNC HERE i I' the developed as ADD B i not the contents of a HUT is Ed of propon. Typut data 2050 : 04+1 2051 : 06+1 in all on creation to the to accompany the · a solo accumulator . 1126 menous ; transfer the quotient stople the remainder A and & to get the Br meniory 9 step: 6 ef there is no covery step : 8 stone the lever byte in menory. 8-ble YOULTIPLICATION the memory location 20541 IT BLOOD OF STEP: 10 Erd. PROGRAM: JDA 2050H: Take the multiplier to step it secrement the s suggister. stogister. STEP:5 stad the multiplies and the strep: 3 Get the multipliend from STEP: 2 save the multiplier to B step: 4 clear a refers to state the NGORITHM: STEP: 1 Get the multiples from the to the accumulator. coccumulation and in that MON BIA : Manyer the multiplier to Nemary lacation 2050 H to the accumulation. B suggester.

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and the states of 87A 2053H MOV AND STA 2052H : shore the lawer byte of A CONT ENR O DCR B JNZ HORE MOU DI X MOV CIA IDA 2051M : take the multiplicard to JNC GOTO ADD C I XRA A : Asiantfex the multiplicard to is of there is no carry, ton : clear o suggister to stope the c.} s iclear the accumulation . : of the value in B register is : Add the contents of A and c account the suggester by the location named HERE . product in memory. accumulator . c seglistor . out equal to zero, then jump to strone the higher late or monuzy. carry . one white it is stated go to the location ramed registers and a part trid of propriam. when one NON DIVIN 6 stepp", save the first number in 8 register. MOV B, A: Transfer the first junter lite B. 10A 2051H 3 take the second jumber (minuend) 2052H v Example: Anput data: 2050:43 Step 5 : shale the difference with is in STEPS: Fid. - stalling 3 to allow steph ? Subbact the numbers by n and B. memory location 2051 to the acumulation. steps: Get the second runnes from the memory location posets to the occumulator. 8-bet subraction : Example in a single of the first drumber (subabad) caccumulation in the memory lacation ALGORNTHM 5step1: but the first number from the sub B : subtract the first runner farm Result ? 2052 : 05 N. C. S. C. S. S. the second kumber. 205 1 204 2053 : 0]

| Example : anyur ann : soso: 49 (subtrated) software : 2052 : 32 Algorence : 2052 : 32 Algorenthe: srep : adultative H1 pair an monoral polidion or p2 : adultative the monoral H2 or en- steps : sociement the monoral H4 or en- tor. srep : sociement the monoral H4 or en- anter the data is is sequere. or step 1: or step 1: or step 1: or p2 : the data is is sequere. sreps : then also be sequere. or step 1: or step 1: or p2 : the stand is be sequere. second data stand is be sequere. Second data stand is a menoral. | STA 2052 H : Shope the difference & memory, HLT : ed & pargram.» |
|---|---|
| | steplo: Decrement court in register & by one. |

| 2056:21 2057:26 2057:26 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2059:20 2051:2 | 2050; 2A 2050; 2A 2051; FF 20552:03 2055; IC 2054:32 2054:32 2054:32 | HLT; End & program. HLT; End & program. Example: Example: | JNZ 10092; In 10092. and plat up the inequal RCR c; becoment the c englister by one, to place, the indepest form the demainder. JNZ 10093; doto and continue this confister | Nov MA; Else 'surp' first data and second. DCXH : data storred & memory. Mov MIB : INV H : Restare unenwey address INV H : Restare unenwey address INV H : Restare unenwey address |
|---|--|--|---|---|
| SA SOSI; stople the program. | HLT HLT APPER modicia's by add the desired address with the mit the big all and to some the | 2x I HI 5000; Initialize Look up table address 1DA 2050; Bet the data CPI ON ; check light sq JC AFTER; Example and/catlon; | steps: it yos go to near step as delse halt the pergenam. steps: and the desired address with the accumulation content. steps: Stone the stocult. | SQUARE OF A NUMBER VEING FOR UP TABLE; ALGORITTHM! STEP1! TABLEALIZE HI Pala to polat look up STEP2: Get the data. STEP3: Check whether the give loput is less thousa. |

.

| STEPS: compare the data in A suggister with the data in B seglister. | to accumulation. STEPA: Increment inerviewy address in this STEP 5 3 More the second data from menuoy to a sneglister. | STEP1: Enditalize HI pair which stopies to rumbers. STEP3: Get drie caut to c stepfiston. STEP3: Move the forst data, from monocey | a) LARGEET - SMALLEET + 1 100 Malaatien) in memory | ANDER DARA : 1/4 & memory location soes | 500% AU 500% AU | 5000 cm 5002 09 5005 36 | |
|---|---|--|--|---|-----------------------|---|--|
| May Mile : Any H : Restage menuscip addresss: | 6 | Mov B/M of the second number to B englisher. In the second number to B and ful and shape the data in A and B and ful and shape the data in A and B | x x | | to zono go to step 3. | steps: the stand is moment. greps: Decrement cant sugester chipme. | |

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10) MULTIBYTE ADDITION + steps , rod MT segister pale with monory ANZLOOPZ; arculture & woop2. Loop 1 , DCR , the comparisons are not over. Ac to the location HERE when a voir voir fruncier of bytes principale with step 8 : " décement utions preglister layone. PROGRAM ! step # : increment the polynoss by me step a: af the trangister content is zero, STEPH: wood the oregester part of monoacy is a STEPS & Stasse the sesult in the menand. step 2: Get the caut to c segester with KRA A: dear the accumulation and ertep1: cleans accumulation and casery blog. STEPS: trajee the encor byte ento the locarlen 20504, unexe first data is suped. ALGORHTHM?: location solotty, where second atta is shored. nex H : obtain strated by memory. and de partes. althout a turt. a same of ophics of another or the country. stored. unitope address its 205014. memory address 20604 Drub the accumulator. umenuous addresso universe the second data is 1xt 0,2060H; road the se elegister pair with the the second mathematical and the second s shared . MUT CIOLH : 2000 the called with the number. not zero, then from to the location round HERE. momorely address where the first due is 1× I Dr 2000H ; 2000 the HL everylester pair with that cheves trace age a sedance with we INVED ; Increment the address in the segment. NOC M; nod with carry, the content of the accumulance with the syte in the IN Z HERE; of the content of the c stepleten is of whites a sequence of the counter. one. mennery address in 2050H and and star mov min ; state the sesuit in the menally ocr c ; recomment the c suglister content by INX H , on demont the address on HI suggester fri Cur a - (s.) -

ID NUTIBLIE SUBTRACTION 'S COMPANY IN THE WAY snepli : thorement the c singlister content by Suc . STEP 3. Lood HI magester with mendery location. STEP123 af the content is not zero, go to step 10: and the ac address by STEP 43 2000H Juneal forst data 28' stored . stop 5. STEPT 11 isub with boordow steps 3: Load the register pair in monagy steps: Get the court to a register with a ALCORITHM'S PROVERAM & steps: nake the law white but accumulators step1; closs the accumulation and courty fleg. step 9: Increment the HI deglover address location second, uneve second data la starved. mumber of dytes is suggester to the counter. STEPS: above the everyt in the metally. by one. step13 : end. trag-MUE C, OCH; Load whe c sequeter with the XRA A; clear the accumulation and accery

Is stored. shored. unemary address where the second data is with monory address where the fort data menuscy address where the second data & IND DIDOGH ; load the to elegister pile with should 10AX &' take the lower byte from the monicely address second in the accumulated. INCO ; Druement the address in DE register memory address 2050 from the content of by one. 3BB M; sub with bourdy, the byte in the by one. occumulatost . oce c', becoment the c register untert by one. INX H ; indement the address in HI suglister whose address is socout. now min ; showe the result in the memory INZHERS; of the content of a explorer is not zero, then Jump to the location named HERE . HLT , End of program, road the os register bals with

1×I HJ2050H ; Load the HL elegister palse

EXAMPLE ! INPUT DATA: RESULT: Charles Startes 2050:03 2050:EB - 12 2051 :73 2051: CF : 2052:6D 2052": 21 Sales a land per states : tout de la martine ver interior, district autors and the interior data it 120 100 of the said way and a to said 6) Evaluate: 89a) 89H + 14H -89H + 14H = 9DH $\frac{14}{9D}$ 9<u>0</u> 6) 51H-19H 4881 51H-19H = 38H . 19 March is contrated where a pricipian to stars databyte 52H Bito 5) memory location 5000H, 12 2 12 STOKED THERE AND A CROSSING ON THE ONDIVISION - 300 jul there is surrout the couple ending 1 3m 14 the of antipole of the methods of a cooperation in PRIOR DECK IN TOTAL COMMENTS