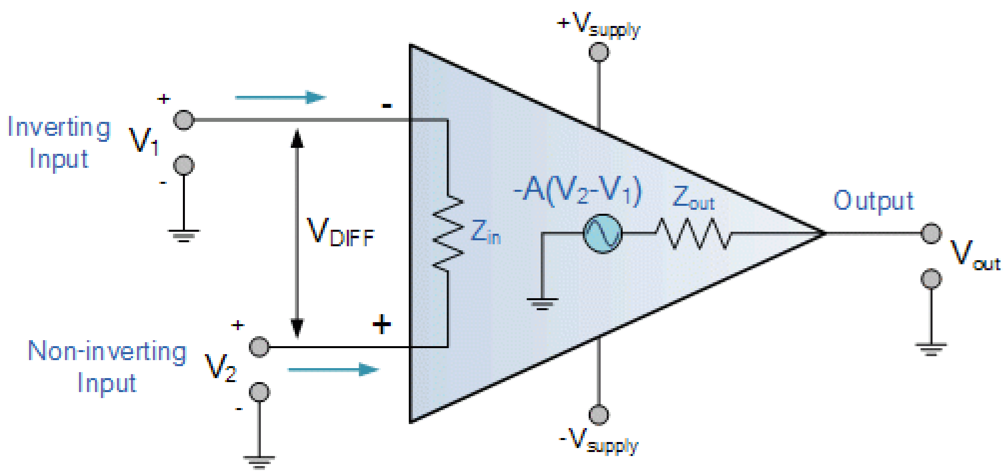


Operational Amplifier Basics

Operational Amplifiers, or **Op-amps** as they are more commonly called, are one of the basic building blocks of Analogue Electronic Circuits.

Operational amplifiers are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation.

An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the **Inverting Input**, marked with a negative or "minus" sign, (−). The other input is called the **Non-inverting Input**, marked with a positive or "plus" sign (+).

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

Voltage – Voltage "in" and Voltage "out"

Current – Current "in" and Current "out"

Transconductance – Voltage "in" and Current "out"

Transresistance – Current "in" and Voltage "out"

Since most of the circuits dealing with operational amplifiers are voltage amplifiers, we will limit the tutorials in this section to voltage amplifiers only, (Vin and Vout).

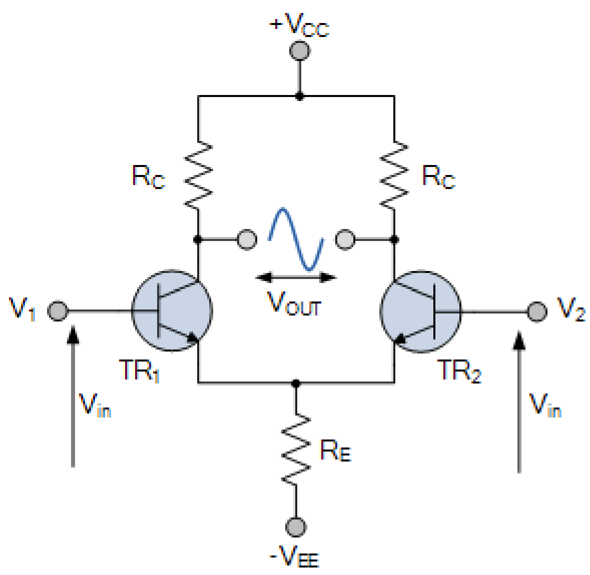
The output voltage signal from an Operational Amplifier is the difference between the signals being applied to its two individual inputs. In other words, an op-amps output signal is the difference between the two input signals as the input stage of an Operational Amplifier is in fact a differential amplifier as shown below.

Differential Amplifier

The circuit below shows a generalized form of a differential amplifier with two inputs marked V1 and V2. The two identical transistors TR1 and TR2 are both biased at the same operating point with their emitters connected together and returned to the common rail, -Vee by way of resistor Re.

The circuit operates from a dual supply +Vcc and -Vee which ensures a constant supply. The voltage that appears at the output, Vout of the amplifier is the difference between the two input signals as the two base inputs are in *anti-phase* with each other.

So as the forward bias of transistor, TR1 is increased, the forward bias of transistor TR2 is reduced and vice versa. Then if the two transistors are perfectly matched, the current flowing through the common emitter resistor, Re will remain constant.



Differential Amplifier

Like the input signal, the output signal is also balanced and since the collector voltages either swing in opposite directions (anti-phase) or in the same direction (in-phase) the output voltage signal, taken from between the two collectors is, assuming a perfectly balanced circuit the zero difference between the two collector voltages.

This is known as the *Common Mode of Operation* with the **common mode gain** of the amplifier being the output gain when the input is zero.

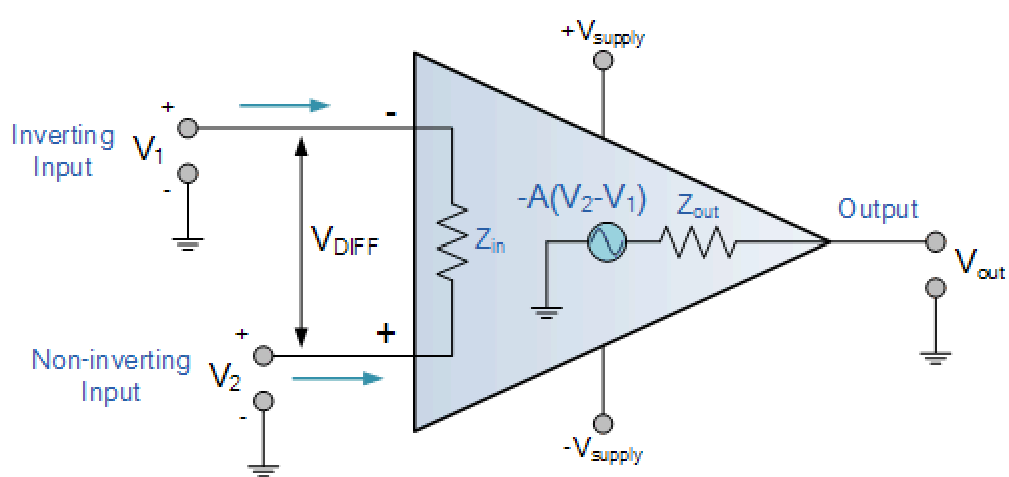
Operational Amplifiers also have one output (although there are ones with an additional differential output) of low impedance that is referenced to a common ground terminal and it should ignore any common mode signals that is, if an identical signal is applied to both the inverting and non-inverting inputs there should no change to the output.

However, in real amplifiers there is always some variation and the ratio of the change to the output voltage with regards to the change in the common mode input voltage is called the **Common Mode Rejection Ratio** or **CMRR** for short.

Operational Amplifiers on their own have a very high open loop DC gain and by applying some form of **Negative Feedback** we can produce an operational amplifier circuit that has a very precise gain characteristic that is dependant only on the feedback used. Note that the term "open loop" means that there are no feedback components used around the amplifier so the feedback path or loop is open.

An operational amplifier only responds to the difference between the voltages on its two input terminals, known commonly as the "*Differential Input Voltage*" and not to their common potential. Then if the same voltage potential is applied to both terminals the resultant output will be zero. An Operational Amplifiers gain is commonly known as the **Open Loop Differential Gain**, and is given the symbol (A_o).

Equivalent Circuit of an Ideal Operational Amplifier



Op-amp Parameter and Idealised Characteristic

Open Loop Gain, (Avo)

Infinite – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for such an amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.

Input impedance, (Z_{IN})

Infinite – Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry ($I_{IN} = 0$). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.

Output impedance, (Z_{OUT})

Zero – The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output impedances in the 100-20kΩ range.

Bandwidth, (BW)

Infinite – An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

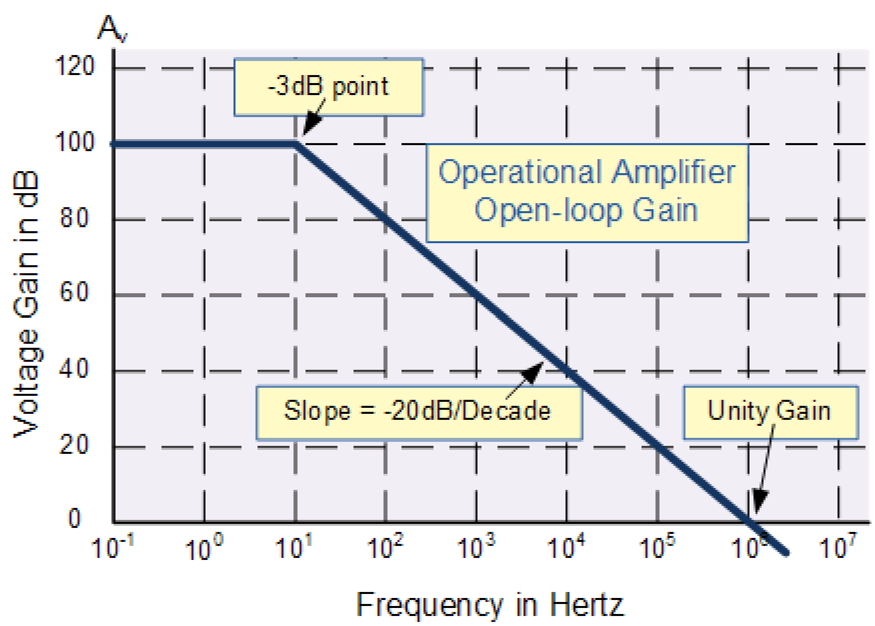
Offset Voltage, (V_{IO})

> **Zero** – The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

From these "idealized" characteristics above, we can see that the input resistance is infinite, so **no current flows into either input terminal** (the "current rule") and that the **differential input offset voltage is zero** (the "voltage rule"). It is important to remember these two properties as they will help us understand the workings of the **Operational Amplifier** with regards to the analysis and design of op-amp circuits.

However, real **Operational Amplifiers** such as the commonly available **uA741**, for example do not have infinite gain or bandwidth but have a typical "Open Loop Gain" which is defined as the amplifiers output amplification without any external feedback signals connected to it and for a typical operational amplifier is about 100dB at DC (zero Hz). This output gain decreases linearly with frequency down to "Unity Gain" or 1, at about 1MHz and this is shown in the following open loop gain response curve.

Open-loop Frequency Response Curve

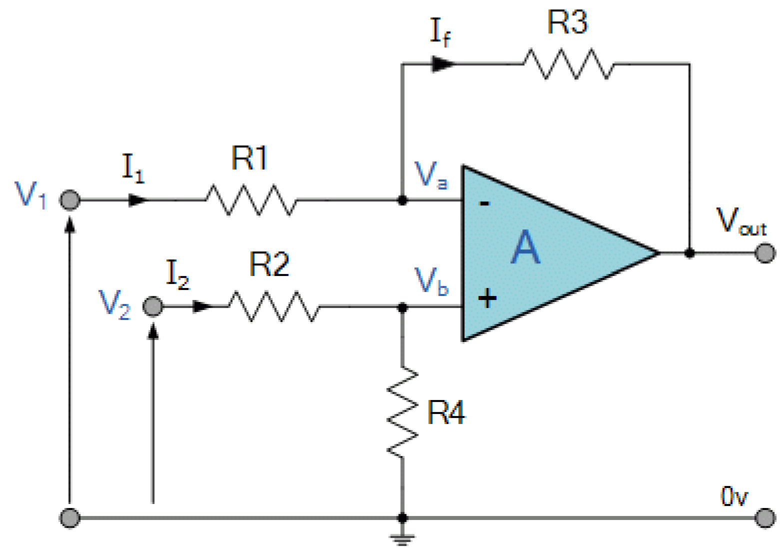


From this frequency response curve we can see that the product of the gain against frequency is constant at any point along the curve. Also that the unity gain (0dB) frequency also determines the gain of the amplifier at any point along the curve. This constant is generally known as the **Gain Bandwidth Product** or **GBP**. Therefore:

$$GBP = \text{Gain x Bandwidth} = A \times BW$$

For example, from the graph above the gain of the amplifier at 100kHz is given as 20dB or 10, then the gain bandwidth product is calculated as:

$$GBP = A \times BW = 10 \times 100{,}000\text{Hz} = 1{,}000{,}000.$$



The Differential Amplifier

The differential amplifier amplifies the voltage difference present on its inverting and non-inverting inputs

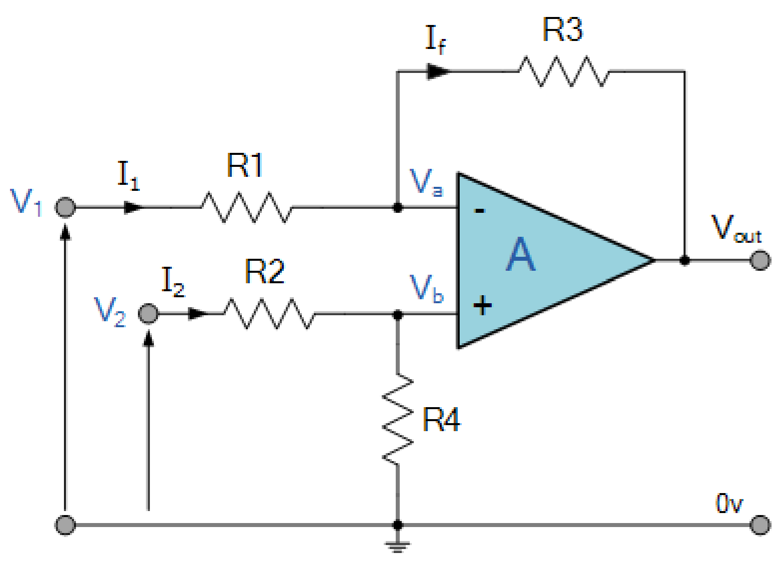
Thus far we have used only one of the operational amplifiers inputs to connect to the amplifier, using either the "inverting" or the "non-inverting" input terminal to amplify a single input signal with the other input being connected to ground.

But as a standard operational amplifier has two inputs, inverting and no-inverting, we can also connect signals to both of these inputs at the same time producing another common type of operational amplifier circuit called a **Differential Amplifier**.

Basically, as we saw in the first tutorial about operational amplifiers, all op-amps are "Differential Amplifiers" due to their input configuration. But by connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to the "Difference" between the two input voltage signals of V_1 and V_2.

Then *differential amplifiers* amplify the difference between two voltages making this type of operational amplifier circuit a **Subtractor** unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a **Differential Amplifier** configuration and is shown below:

Differential Amplifier



By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage Vout. Then the transfer function for a **Differential Amplifier** circuit is given as:

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } \; V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

Differential Amplifier Equation

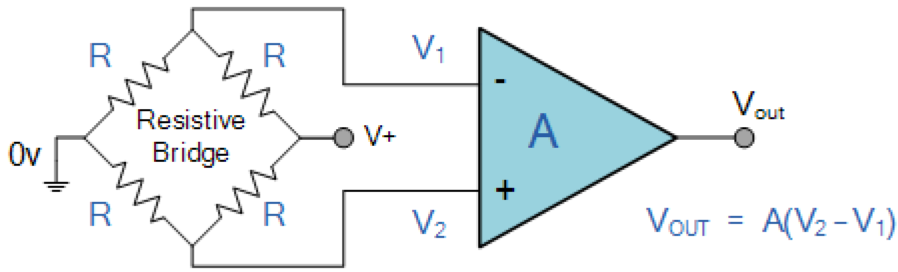
$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = $V_2 - V_1$.

Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive.

The **Differential Amplifier** circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors R1 and R3, the resultant circuit can be made to either "Add" or "Subtract" the voltages applied to their respective inputs. One of the most common ways of doing this is to connect a "Resistive Bridge" commonly called a *Wheatstone Bridge* to the input of the amplifier as shown below.

Wheatstone Bridge Differential Amplifier



The standard Differential Amplifier circuit now becomes a differential voltage comparator by "Comparing" one input voltage to the other. For example, by connecting one input to a fixed voltage reference set up on one leg of the resistive bridge network and the other to either a "Thermistor" or a "Light Dependant Resistor" the amplifier circuit can be used to detect either low or high levels of temperature or light as the output voltage becomes a linear function of the changes in the active leg of the resistive bridge and this is demonstrated below.

Light Activated Differential Amplifier

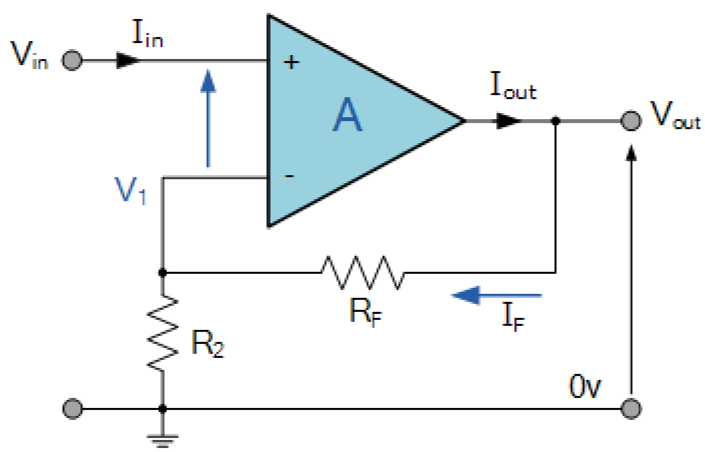
Non-inverting Operational Amplifier

The second basic configuration of an operational amplifier circuit is that of a **Non-inverting Operational Amplifier** design.

In this configuration, the input voltage signal, (V_{IN}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (−) input terminal via a $Rf - R2$ voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, $Rout$ as shown below.

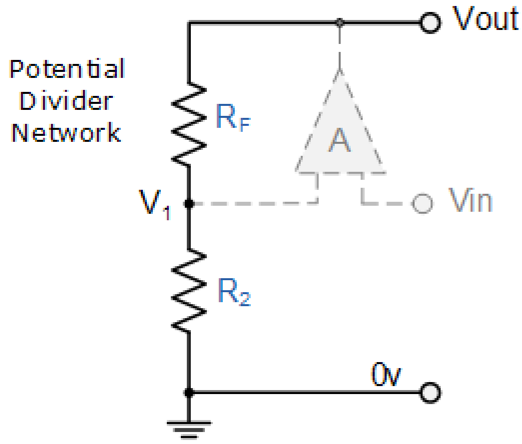
Non-inverting Operational Amplifier Configuration



In the previous Inverting Amplifier tutorial, we said that for an ideal op-amp "No current flows into the input terminal" of the amplifier and that "V1 always equals V2". This was because the junction of the input and feedback signal (V1) are at the same potential.

In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, Rf and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and Rf as shown below.

Equivalent Potential Divider Network



Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A_V) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

$$\text{Ideal Summing Point: } V_1 = V_{IN}$$

$$\text{Voltage Gain, } A_{(V)} \text{ is equal to: } \frac{V_{OUT}}{V_{IN}}$$

$$\text{Then, } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$$

$$\text{Transpose to give: } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$$

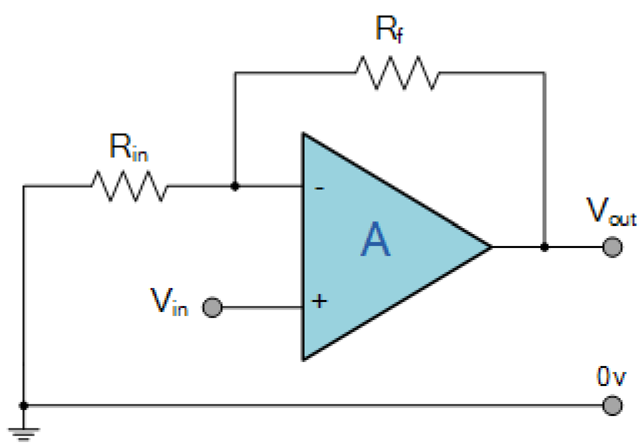
Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

$$A_{(v)} = 1 + \frac{R_F}{R_2}$$

We can see from the equation above, that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of R*f* and R2.

If the value of the feedback resistor R*f* is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor R2 is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, (A_O).

We can easily convert an inverting operational amplifier configuration into a non-inverting amplifier configuration by simply changing the input connections as shown.



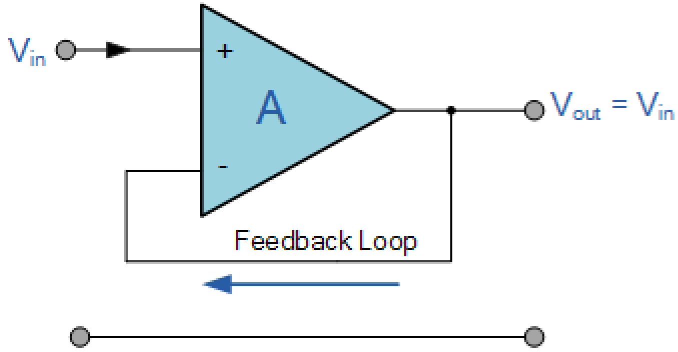
Voltage Follower (Unity Gain Buffer)

If we made the feedback resistor, R*f* equal to zero, (R*f* = 0), and resistor R2 equal to infinity, (R2 = ∞), then the resulting circuit would have a fixed gain of "1" (unity) as all the output voltage is fed back to the inverting input terminal (negative feedback). This configuration would produce a special type of the non-inverting amplifier circuit called a **Voltage Follower**, also known as a "unity gain buffer".

As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, thus Vout = Vin. This then makes the **voltage follower** circuit ideal as a constant voltage source or voltage regulator because of its input to output isolation properties.

The advantage of the unity gain voltage follower configuration is that it can be used when impedance matching or circuit isolation is more important than voltage or current amplification as it maintains the input signal voltage at its output terminal. Also, the input impedance of the voltage follower circuit is extremely high, typically above 1MΩ as it is equal to that of the operational amplifiers input resistance times its gain (Rin x A_O). The op-amps output impedance is very low since an ideal op-amp condition is assumed so is unaffected by changes in load.

Non-inverting Voltage Follower



In this non-inverting circuit configuration, the input impedance Rin has increased to infinity and the feedback impedance Rf reduced to zero. The output is connected directly back to the negative inverting input so the feedback is 100% and Vin is exactly equal to Vout giving it a fixed gain of 1 or unity. As the input voltage Vin is applied to the non-inverting input, the voltage gain of the amplifier is therefore given as:

$$V_{out} = A(V_{in})$$

$$(V_{in} = V+) \text{ and } (V_{out} = V-)$$

$$\text{therefore Gain, } (A_V) = \frac{V_{out}}{V_{in}} = +1$$

Since no current flows into the non-inverting input terminal the input impedance is infinite (ideal conditions) so zero current will flow through the feedback loop. Thus any value of resistance may be placed in the feedback loop without affecting the characteristics of the circuit as no current flows through it so there is zero voltage drop across it resulting in zero power loss.

As the input impedance is extremely high, the unity gain buffer (voltage follower) can be used to provide a large power gain as the extra power comes from the op-amps supply rails and through the op-amps output to the load and not directly from the input. However in most real unity gain buffer circuits there are leakage currents and parasitic capacitances present so a low value (typically 1kΩ) resistor is required in the feedback loop to help reduce the effects of these leakage currents providing stability especially if the operational amplifier is of a current feedback type.

The voltage follower or unity gain buffer is a special and very useful type of **Non-inverting amplifier** circuit that is commonly used in electronics to isolated circuits from each other especially in High-order state variable or Sallen-Key type active filters to separate one filter stage from the other. Typical digital buffer IC's available are the 74LS125 Quad 3-state buffer or the more common 74LS244 Octal buffer.

One final thought, the closed loop voltage gain of a voltage follower circuit is "1" or **Unity**. The open loop voltage gain of an operational amplifier with no feedback is **Infinite**. Then by carefully selecting the feedback components we can control the amount of gain produced by a non-inverting operational amplifier anywhere from one to infinity.

Thus far we have analysed an inverting and non-inverting amplifier circuit that has just one input signal, Vin. In the next tutorial about Operational Amplifiers, we will examine the effect of the output voltage, Vout by connecting more inputs to the amplifier. This then produces another common type of operational amplifier circuit called a Summing Amplifier which can be used to "add" together the voltages present on its inputs.

124 Comments

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A

Abubakari Marwan

No comment

Posted on August 08th 2021 | 9:38 am

Reply

W

waleed jamal

design an op amp based on inverting amplifier to provide a minimum gain of 10 to an input signal of 100khz and peak voltage and peak voltage of 25mV ,whereas the input impedence of should not be less than 10k ohm ,select the op-amp application to be used i.e unity gain bandwidth and slew rate,also decide the value of input voltage and draw cicuit diagrame

Posted on June 02nd 2021 | 5:28 pm

Reply

Daniel McErlain

Gud circut me likke aloot

Posted on March 24th 2021 | 9:45 am

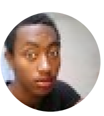
Reply

Mutsa Chitagu

Well explained , short and precise notes

Posted on March 12th 2021 | 12:02 pm

Reply



Daniel Fikadu

ok thanks for your .....t..rial

Posted on February 18th 2021 | 7:09 pm

Reply

Girish s

Elevtron

Posted on February 13th 2021 | 1:48 am

Reply

P

Prssanna CJ

I want to know more about Operational amplifiers and comparators

Posted on January 18th 2021 | 4:59 pm

Reply

T

Thomas J Walker

How to best simulate a gain 1.5 Vdc in ltspice

Posted on January 16th 2021 | 9:52 am

Reply

S

sir hassas

this is very useful
thanks

Posted on November 18th 2020 | 7:57 am

Reply

A

Abyr

Luna – satellite of Earth.

Posted on September 11th 2020 | 10:44 am

Reply

I

I Ketut Wiryajati

Thanks for tutorials, its useful for me, and the best for you,
Are your picture/image have Copyright, and may i use it. thank a lot

Posted on September 09th 2020 | 10:34 pm

Reply

S

Shakeel Ahmad Malik

i like this artical

Posted on September 01st 2020 | 10:23 am

Reply

H

humphrey mulenga

i want to know the opn loop and closed loop theory

Posted on August 03rd 2020 | 12:40 pm

Reply

V

Vo Cuong

Thanks for tutorials, it useful for me

Posted on July 26th 2020 | 2:38 am

Reply

S

Saru

Design and set up inverting and non inverting amplifier for gain 40.plot a input wave form?

Posted on July 23rd 2020 | 7:53 am

Reply

P

petra

how can i make citation or reference for APA style? Can I know the author name.

Posted on June 13th 2020 | 7:53 am

Reply

S

SONNE ROBERT

Specify values of resistors and for a non-inverting 741 op-amp amplifier with a gain of 10.
Find the cutoff frequency and the phase shift for a sinusoidal input voltage with a frequency of 10,000 Hz.

Posted on May 09th 2020 | 6:20 pm

Reply

A

Anyangwa Emmanuel

How do I analyze an opam

Posted on February 23rd 2020 | 10:33 am

Reply

N

nanda

what happens if i put a current limiting resistor to the input terminal [non-inverting input terminal]? would its gain get differed slightly?

tell me all the details the gain is varied by…….

looking forward for your answers……………

Posted on December 19th 2019 | 10:07 am

Reply

Inverting Operational Amplifier

The Inverting Operational Amplifier configuration is one of the simplest and most commonly used op-amp topologies

We saw in the last tutorial that the **Open Loop Gain**, (A_{VO}) of an operational amplifier can be very high, as much as 1,000,000 (120dB) or more.

However, this very high gain is of no real use to us as it makes the amplifier both unstable and hard to control as the smallest of input signals, just a few micro-volts, (μV) would be enough to cause the output voltage to saturate and swing towards one or the other of the voltage supply rails losing complete control of the output.

As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

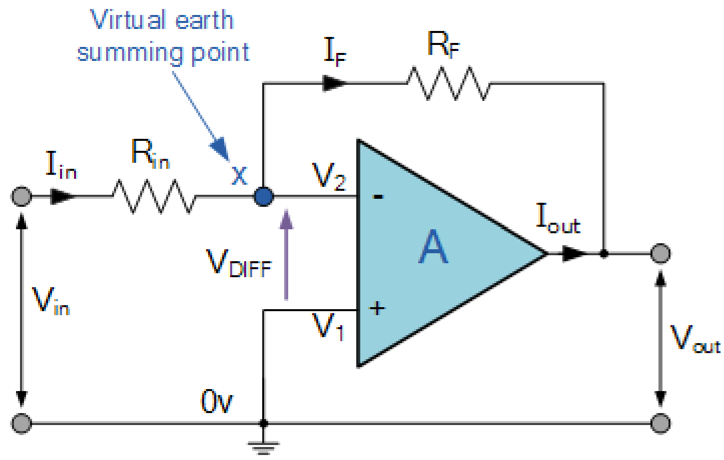
Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external **Feedback Resistor** called $Rƒ$. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain.

This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a *Summing Point*. We must therefore separate the real input signal from the inverting input by using an **Input Resistor**, Rin.

As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a *Virtual Earth* summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a "differential amplifier".

Inverting Operational Amplifier Configuration



In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken.

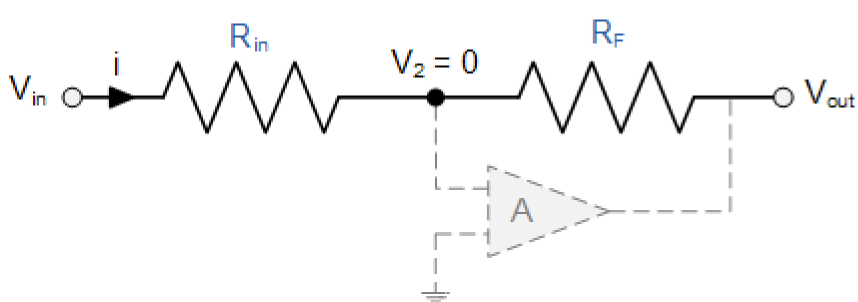
This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **"Virtual Earth"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.

> No Current Flows into the Input Terminals
>
> The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.

Current (i) flows through the resistor network as shown.



$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

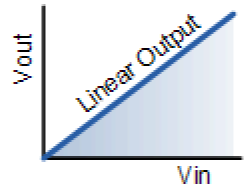
$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

and this can be transposed to give Vout as:

$$Vout = -\frac{Rf}{Rin} \times Vin$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180^{o} out of phase. This is due to the feedback being negative in value.

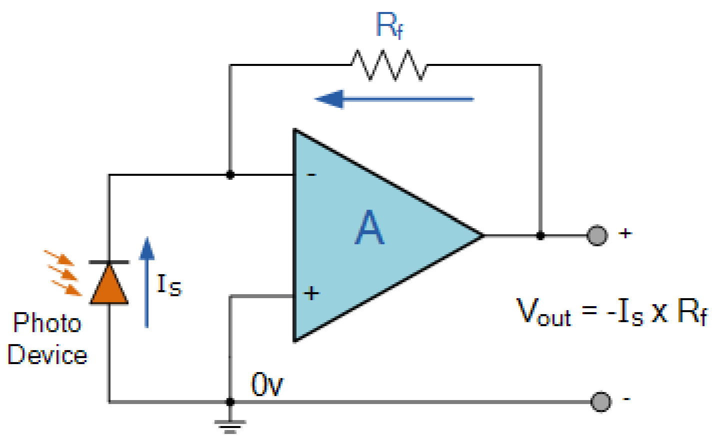
The equation for the output voltage Vout also shows that the circuit is linear in nature for a fixed amplifier gain as Vout = Vin x Gain. This property can be very useful for converting a smaller sensor signal to a much larger voltage.



Linear Output

Another useful application of an inverting amplifier is that of a "transresistance amplifier" circuit. A **Transresistance Amplifier** also known as a "transimpedance amplifier", is basically a current-to-voltage converter (Current "in" and Voltage "out"). They can be used in low-power applications to convert a very small current generated by a photo-diode or photo-detecting device etc, into a usable output voltage which is proportional to the input current as shown.

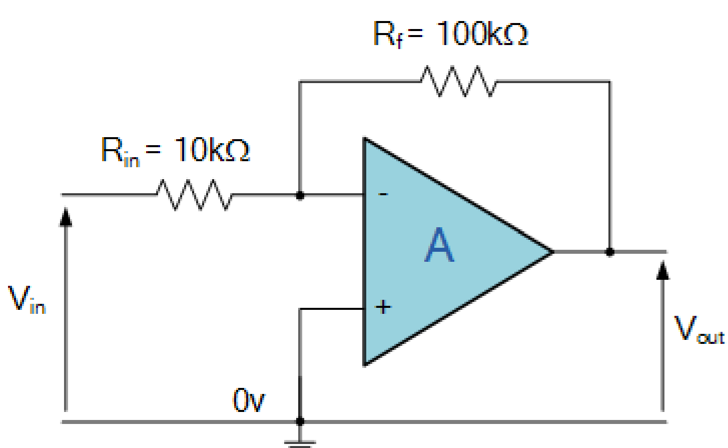
Transresistance Amplifier Circuit



The simple light-activated circuit above, converts a current generated by the photo-diode into a voltage. The feedback resistor Rf sets the operating voltage point at the inverting input and controls the amount of output. The output voltage is given as Vout = I_S x Rf. Therefore, the output voltage is proportional to the amount of input current generated by the photo-diode.

Inverting Op-amp Example No1

Find the closed loop gain of the following inverting amplifier circuit.



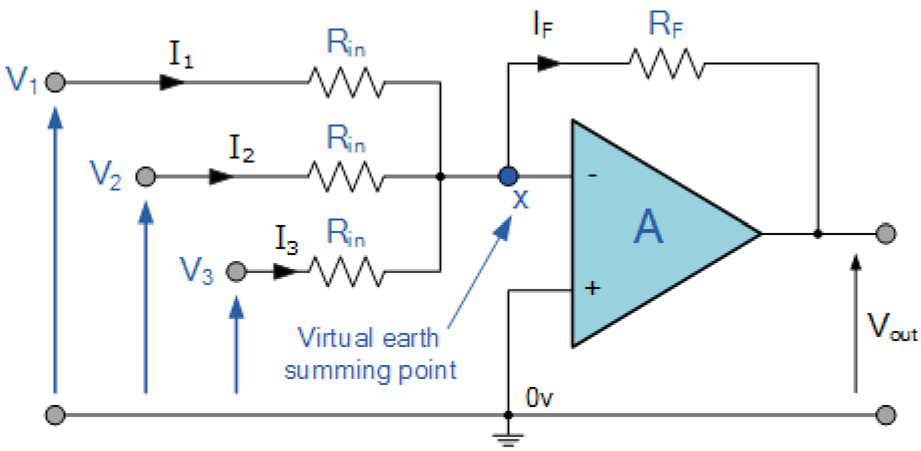
Using the previously found formula for the gain of the circuit

The Summing Amplifier

The **Summing Amplifier** is another type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage.

We saw previously in the inverting operational amplifier that the inverting amplifier has a single input voltage, (Vin) applied to the inverting input terminal. If we add more input resistors to the input, each equal in value to the original input resistor, (Rin) we end up with another operational amplifier circuit called a **Summing Amplifier**, "*summing inverter*" or even a "*voltage adder*" circuit as shown below.

Summing Amplifier Circuit



In this simple summing amplifier circuit, the output voltage, (Vout) now becomes proportional to the sum of the input voltages, V_1, V_2, V_3, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, (R_{IN}) are equal in value, we can simplify the above equation to give an output voltage of:

Summing Amplifier Equation

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots.etc\right)$$

We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltages V_1, V_2 and V_3. We can also add more inputs if required as each individual input "sees" their respective resistance, Rin as the only input impedance.

This is because the input signals are effectively isolated from each other by the "virtual earth" node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and Rf is equal to Rin.

Note that when the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.

A **Scaling Summing Amplifier** can be made if the individual input resistors are "NOT" equal. Then the equation would have to be modified to:

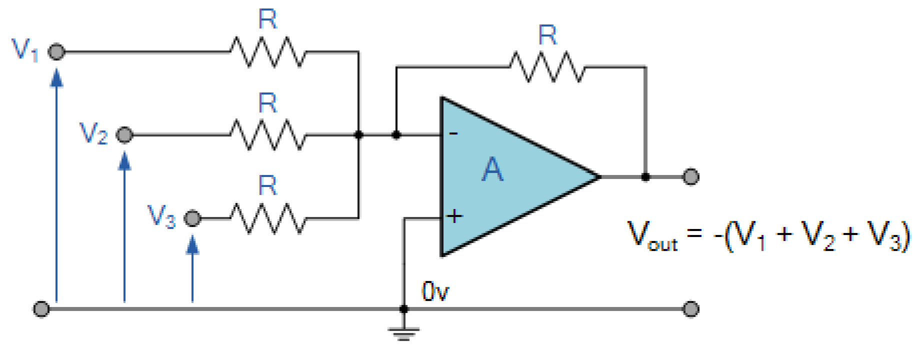
$$-V_{OUT} = V_1\left(\frac{R_f}{R_1}\right) + V_2\left(\frac{R_f}{R_2}\right) + V_3\left(\frac{R_f}{R_3}\right) \text{....etc}$$

To make the math's a little easier, we can rearrange the above formula to make the feedback resistor R*f* the subject of the equation giving the output voltage as:

$$-V_{OUT} = R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \text{....etc}$$

This allows the output voltage to be easily calculated if more input resistors are connected to the amplifiers inverting input terminal. The input impedance of each individual channel is the value of their respective input resistors, ie, R_1, R_2, R_3 ... etc.

Sometimes we need a summing circuit to just add together two or more voltage signals without any amplification. By putting all of the resistances of the circuit above to the same value R, the op-amp will have a voltage gain of unity and an output voltage equal to the direct sum of all the input voltages as shown:

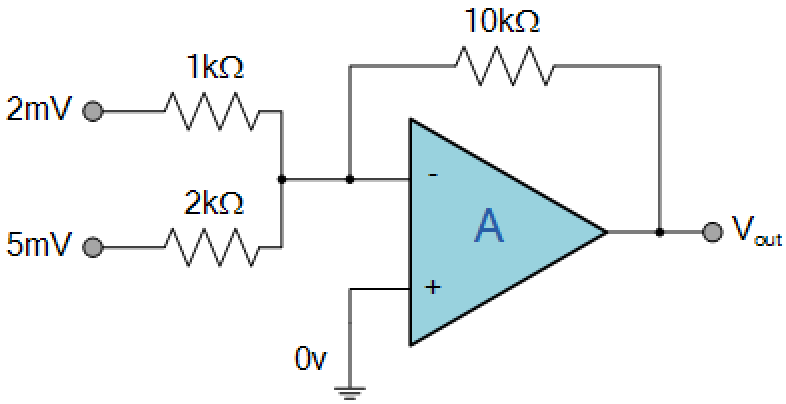


The **Summing Amplifier** is a very flexible circuit indeed, enabling us to effectively "Add" or "Sum" (hence its name) together several individual input signals. If the inputs resistors, R_1, R_2, R_3 etc, are all equal a "unity gain inverting adder" will be made. However, if the input resistors are of different values a "scaling summing amplifier" is produced which will output a weighted sum of the input signals.

Summing Amplifier Example No1

Find the output voltage of the following *Summing Amplifier* circuit.

Summing Amplifier



Using the previously found formula for the gain of the circuit:

$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

We can now substitute the values of the resistors in the circuit as follows:

$$A_1 = \frac{10k\Omega}{1k\Omega} = -10$$

$$A_2 = \frac{10k\Omega}{2k\Omega} = -5$$

We know that the output voltage is the sum of the two amplified input signals and is calculated as:

$$Vout = (A_1 \times V_1) + (A_2 \times V_2)$$

$$Vout = (-10(2mV)) + (-5(5mV)) = -45mV$$

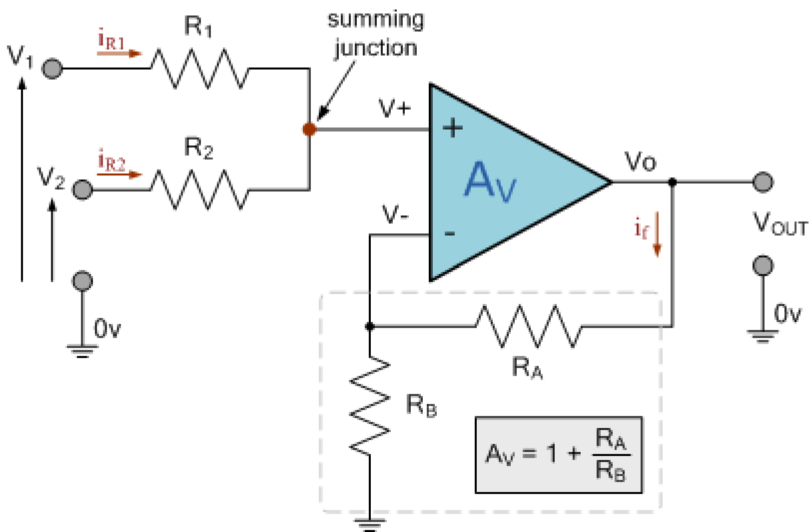
Then the output voltage of the **Summing Amplifier** circuit above is given as **-45 mV** and is negative as its an inverting amplifier.

Non-inverting Summing Amplifier

But as well as constructing inverting summing amplifiers, we can also use the non-inverting input of the operational amplifier to produce a *non-inverting summing amplifier*. We have seen above that an inverting summing amplifier produces the negative sum of its input voltages then it follows that the non-inverting summing amplifier configuration will produce the positive sum of its input voltages.

As its name implies, the non-inverting summing amplifier is based around the configuration of a non-inverting operational amplifier circuit in that the input (either ac or dc) is applied to the non-inverting (+) terminal, while the required negative feedback and gain is achieved by feeding back some portion of the output signal (V_{OUT}) to the inverting (-) terminal as shown.

Non-inverting Summing Amplifier



So what's the advantage of the non-inverting configuration compared to the inverting summing amplifier configuration. Besides the most obvious fact that the op-amps output voltage V_{OUT} is in phase with its input, and the output voltage is the weighted sum of all its inputs which themselves are determined by their resistance ratios, the biggest advantage of the non-inverting summing amplifier is that because there is no virtual earth condition across the input terminals, its input impedance is much higher than that of the standard inverting amplifier configuration.

Also, the input summing part of the circuit is unaffected if the op-amps closed-loop voltage gain is changed. However, there is more maths involed in selecting the weighted gains for each individual input at the summing junction especially if there are more than two inputs each with a different weighting factor. Nevertheless, if all the inputs have the same resistive values, then the maths involved will be a lot less.

If the closed-loop gain of the non-inverting operational amplifier is made equal the number of summing inputs, then the op-amps output voltage will be exactly equal to the sum of all the input voltages. That is for a two input non-inverting summing amplifier, the op-amps gain is equal to 2, for a three input summing amplifier the op-amps gain is 3, and so on. This is because the currents which flow in each input resistor is a function of the voltage at all its inputs. If the input resistances made all equal, ($R_1 = R_2$) then the circulating currents cancel out as they can not flow into the high impedance non-inverting input of the op-amp and the voutput voltage becomes the sum of its inputs.

So for a 2-input non-inverting summing amplifier the currents flowing into the input terminals can be defined as:

$$I_{R1} + I_{R2} = 0 \quad (KCL)$$

$$\frac{V_1 - V+}{R_1} + \frac{V_2 - V+}{R_2} = 0$$

$$\therefore \left(\frac{V_1}{R_1} - \frac{V+}{R_1} \right) + \left(\frac{V_2}{R_2} - \frac{V+}{R_2} \right) = 0$$

If we make the two input resistances equal in value, then $R_1 = R_2 = R$.

$$V+ = \frac{\frac{V_1}{R} + \frac{V_2}{R}}{\frac{1}{R} + \frac{1}{R}} = \frac{\frac{V_1 + V_2}{R}}{\frac{2}{R}}$$

$$\text{Thus} \quad V+ = \frac{V_1 + V_2}{2}$$

The standard equation for the voltage gain of a non-inverting summing amplifier circuit is given as:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{V+} = 1 + \frac{R_A}{R_B}$$

$$\therefore \quad V_{OUT} = \left[1 + \frac{R_A}{R_B} \right] V+$$

$$\text{Thus:} \quad V_{OUT} = \left[1 + \frac{R_A}{R_B} \right] \frac{V_1 + V_2}{2}$$

The non-inverting amplifiers closed-loop voltage gain A_V is given as: $1 + R_A/R_B$. If we make this closed-loop voltage gain equal to 2 by making $R_A = R_B$, then the output voltage V_O becomes equal to the sum of all the input voltages as shown.

Non-inverting Summing Amplifier Output Voltage

$$V_{OUT} = \left[1 + \frac{R_A}{R_B}\right]\frac{V_1 + V_2}{2}$$

$$\text{If } R_A = R_B$$

$$V_{OUT} = [1+1]\frac{V_1 + V_2}{2} = \cancel{2}\frac{V_1 + V_2}{\cancel{2}}$$

$$\therefore V_{OUT} = V_1 + V_2$$

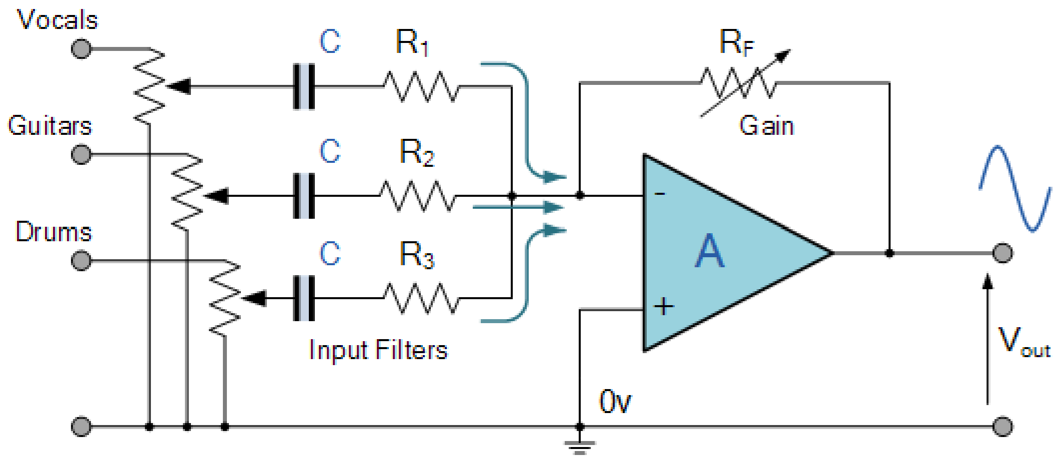
Thus for a 3-input non-inverting summing amplifier configuration, setting the closed-loop voltage gain to 3 will make V_{OUT} equal to the sum of the three input voltages, V_1, V_2 and V_3. Likewise, for a four input summer, the closed-loop voltage gain would be 4, and 5 for a 5-input summer, and so on. Note also that if the amplifier of the summing circuit is connected as a unity follower with R_A equal to zero and R_B equal to infinity, then with no voltage gain the output voltage V_{OUT} will be exactly equal the average value of all the input voltages. That is $V_{OUT} = (V_1 + V_2)/2$.

Summing Amplifier Applications

So what can we use summing amplifiers for, either inverting or non-inverting. If the input resistances of a summing amplifier are connected to potentiometers the individual input signals can be mixed together by varying amounts.

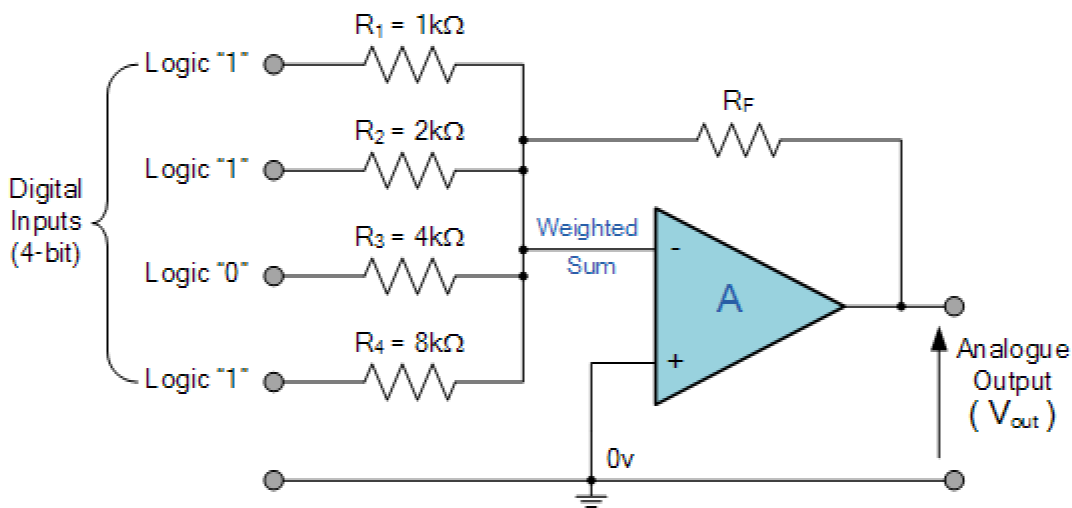
For example, measuring temperature, you could add a negative offset voltage to make the output voltage or display read “0” at the freezing point or produce an audio mixer for adding or mixing together individual waveforms (sounds) from different source channels (vocals, instruments, etc) before sending them combined to an audio amplifier.

Summing Amplifier Audio Mixer



Another useful application of a **Summing Amplifier** is as a weighted sum digital-to-analogue converter, (DAC). If the input resistors, R_{IN} of the summing amplifier double in value for each input, for example, 1kΩ, 2kΩ, 4kΩ, 8kΩ, 16kΩ, etc, then a digital logical voltage, either a logic level "0" or a logic level "1" on these inputs will produce an output which is the weighted sum of the digital inputs. Consider the circuit below.

Digital to Analogue Converter



Of course this is a simple example. In this DAC summing amplifier circuit, the number of individual bits that make up the input data word, and in this example 4-bits, will ultimately determine the output step voltage as a percentage of the full-scale analogue output voltage.

Also, the accuracy of this full-scale analogue output depends on voltage levels of the input bits being consistently 0V for "0" and consistently 5V for "1" as well as the accuracy of the resistance values used for the input resistors, R_{IN}.

Fortunately to overcome these errors, at least on our part, commercially available Digital-to Analogue and Analogue-to Digital devices are readily available with highly accurate resistor ladder networks already built-in.

In the next tutorial about operational amplifiers, we will examine the effect of the output voltage, Vout when a signal voltage is connected to the inverting input and the non-inverting input at the same time to produce another common type of operational amplifier circuit called a Differential Amplifier which can be used to "subtract" the voltages present on its inputs.

101 Comments

bikila

good tutorial, thanks

Posted on April 16th 2021 | 1:08 pm

Reply

Nitesh kumar ram

thank you dear sir

Posted on February 22nd 2021 | 11:32 am

Reply

OSEI- WUSU PHILIP

can you help me with this questions

2. A. An amplifier is represented by the frequency response curve in Figure 2.

i. Determine the band with

ii. The operating frequency

75%

300Hz 2MHz

Figure 2

B. Find the output voltage of the Summing Amplifier circuit shown in Figure 3.

Posted on January 06th 2021 | 10:06 am

Reply

---

mohmmed Alothman

Explain with draw how to use the summing amplifier as a DC shifter to shift an ECG signal with variable gain (from 0.1 to 2.5). Then discuss the most five important parameters of the selected operational amplifier which has been chosen. (

Posted on November 29th 2020 | 11:56 am

Reply

White-Navy

Thanks a lot. So helpful!!!

Posted on November 19th 2020 | 12:48 am

Reply

Lerato Madisha

Thank you, this was very helpful.

Posted on September 02nd 2020 | 3:23 am

Reply

Malik Saad Raees

I want to Design 2-input summing amplifier using a type 741 Op-am, that will sum 3volt (peak-to-peak) + 6volt (peak-to-peak) and give 9volt(peak-to-peak). Set frequency to 300 Hz.
Can anyone help me in this regard please I have one day only?
plz

Posted on July 09th 2020 | 5:44 am

Reply

Ryan

Loving the content here. Wishing there was a little clearer connection between the general case of non inverting op amps and the connection of filters to them. In your DAC example, is the input going to be in terms of impedance from the filter, ie is the capacitance and resistance of the input branch considered with respect to the feedback loop?

Posted on May 08th 2020 | 8:01 pm

Reply

P

Paul

Good tutorial, thanks! And please change “see’s” to “sees”.

Posted on April 25th 2020 | 9:48 am

Reply

S

Stanis

Olá! Muito bom seu tutorial é sua explicação. Como faz pra elaborar um preamp usando amplificador operacional para 4 eletretos?

Posted on April 18th 2020 | 12:22 am

Reply

W

Wayne Storr

No idea, we do not speak Portuguese

Posted on April 18th 2020 | 6:31 am

Reply

F

FELIX NKUMBIRA

good stuff

Posted on March 13th 2020 | 8:12 am

Reply

S

Sylvia

Informative piece.

Posted on March 07th 2020 | 10:21 am

Reply

Iain

I like this

Posted on February 25th 2020 | 12:12 pm

Reply

Daniel Craig

good stuff

Posted on February 25th 2020 | 12:12 pm

Reply

Teshome Ebssa

It is nice website

Posted on February 17th 2020 | 5:54 pm

Reply

SherDil

Thank you very much, Good information in easy and understandable format. Thanks again.

Posted on October 30th 2019 | 5:04 pm

Reply

Akbar

Thanks alot for sharing your knoledge
I have a question about summing amplifer. You explaned inverted summing amplifier but I need a circut for none-inverting summing amplifier.

Posted on October 27th 2019 | 7:32 am

Reply

M

Mistr

Hi Akbar,
If you have a double packed oamp, just use second one as a voltage inverter, then you get a non-inverting summing amplifier.

Posted on October 29th 2019 | 9:54 am

Reply

More

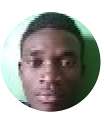
D

Daniel gereziher

It's very interesting.

Posted on September 21st 2019 | 9:49 am

Reply



PAUL AINEBYOONA

This has been my best teacher.
Thanks for the great work guys.

Posted on September 06th 2019 | 11:49 am

Reply

N

Nagaraj

This is the write way to know the summing amplifier explanation

Posted on August 14th 2019 | 2:50 pm

Reply

View More

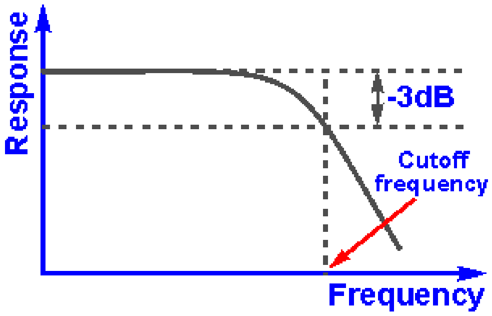
Low pass filter

Active low pass filters can be used for many applications. One area in which these filters can be used is on the output of digital to analogue converters where they are able to remove the high frequency alias components. However they can be used in many other areas where it is necessary to pass the low frequency components of the signal, but remove the unwanted high frequency elements.

Active low pass filters are capable of providing a relatively high level of performance for a small number of components.

What is a low pass filter?

As the name implies, a low pass filter is a filter that passes the lower frequencies and rejects those at higher frequencies.



Low pass filter basic response curve

The shape of the curve is of importance with features like the cut-off frequency and roll off being key to the operation.

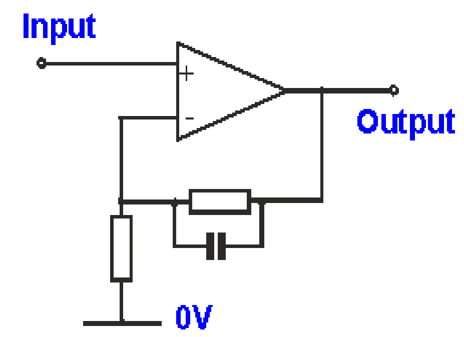
The cut-off frequency is normally taken as the point where the response has fallen by 3dB as shown.

Another important feature is the final slope of the roll off. This is generally governed by the number of 'poles' in the filter. Normally there is one pole for each capacitor inductor in a filter.

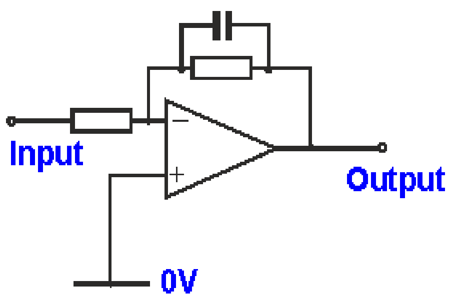
When plotted on a logarithmic scale the ultimate roll-off becomes a straight line, with the response falling at the ultimate roll off rate. This is 6dB per pole within the filter.

Single pole active low pass filter circuit

The simplest circuit low pass filter circuit using an operational amplifier simply places a capacitor across the feedback resistor. This has the effect as the frequency rises of increasing the level of feedback as the reactive impedance of the capacitor falls.



(a) Non-inverting configuration



(b) Inverting configuration

Operational amplifier low pass filter - single pole

The break point for this simple type of filter can be calculated very easily by working out the frequency at which the reactance of the capacitor equals the resistance of the resistor. This can be achieved using the formula:

$$X_c = \frac{1}{2 \pi f C}$$

Where:

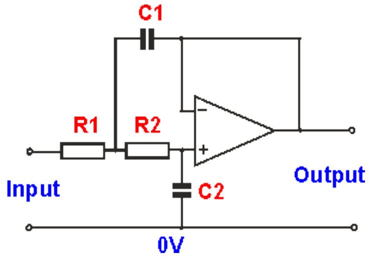
Xc is the capacitive reactance in ohms
Π is the Greek letter and equal to 3.142
f is the frequency in Hertz
C is the capacitance in Farads

The in band gain for these circuits is calculated in the normal way ignoring the effect of the capacitor.

While these operational amplifier circuits are useful to provide a reduction in gain at high frequencies, they only provide an ultimate rate of roll off of 6 dB per octave, i.e. the output voltage halves for every doubling in frequency. This type of filter is known as a one pole filter. Often a much greater rate of rejection is required, and to achieve this it is possible to incorporate a higher performance filter into the feedback circuitry.

Two pole low pass filter op-amp circuit

Although it is possible to design a wide variety of filters with different levels of gain and different roll off patterns using operational amplifiers, the filter described on this page will give a good sure-fire solution. It offers unity gain and a Butterworth response (the flattest response in band, but not the fastest to achieve ultimate roll off out of band).



Operational amplifier two pole low pass filter

Simple sure fire design with Butterworth response and unity gain

The calculations for the circuit values are very straightforward for the Butterworth response and unity gain scenario. Critical damping is required for the circuit and the ratio of the resistor and capacitor values determines this.

$$R1 = R2$$

$$C1 = 2 \times C2$$

$$f = \frac{\sqrt{2}}{4 \pi R C2}$$

When choosing the values, ensure that the resistor values fall in the region between 10 kΩ and 100 kΩ. This is advisable because the output impedance of the circuit rises with increasing frequency and values outside this region may affect the performance.

In particular active high pass filters can be used in many areas to eliminate unwanted signals or general noise.

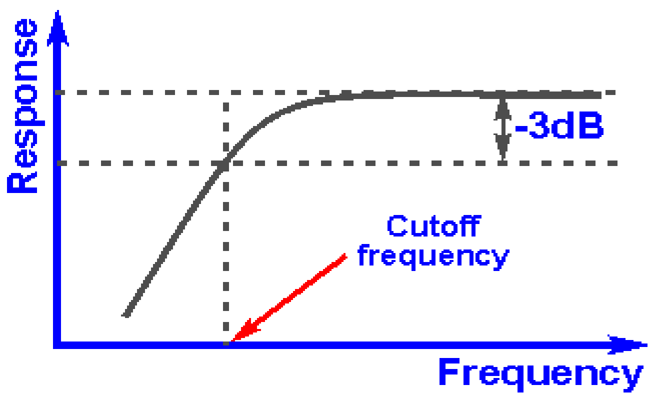
These filters can be used to provide relatively high levels of performance for comparatively few components.

HIGH PASS FILTER

What is a high pass filter?

As the name implies, a high pass filter is a filter that passes the higher frequencies and rejects those at lower frequencies.

This can be used in many instances, for example when needing to reject low frequency noise, hum, etc. from signals. This may be useful in some audio applications to remove low frequency hum, or within RF to remove low frequency signals that are not required.



High pass filter basic response curve

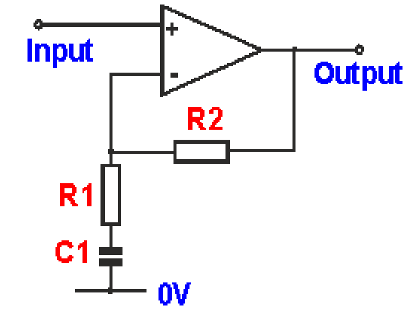
The shape of the curve is of importance. One of the most important features is the cut-off frequency. This is normally taken as the point where the response has fallen by 3dB.

Another important feature is the final slope of the roll off. This is generally governed by the number of 'poles' in the filter. Normally there is one pole for each capacitor inductor in a filter.

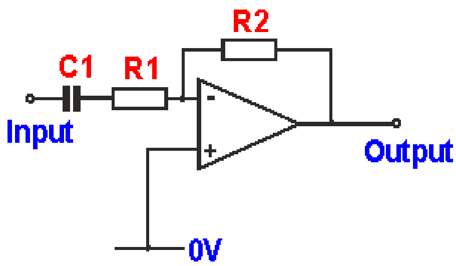
When plotted on a logarithmic scale the ultimate roll-off becomes a straight line, with the response falling at the ultimate roll off rate. This is 6dB per pole within the filter.

Single pole op amp high pass filter

The simplest circuit high pass filter circuit using an operational amplifier can be achieved by placing a capacitor in series with one of the resistors in the amplifier circuit as shown. The capacitor reactance increases as the frequency falls, and as a result this forms a CR low pass filter providing a roll off of 6 dB per octave.



(a) Non-inverting configuration



(b) Inverting configuration

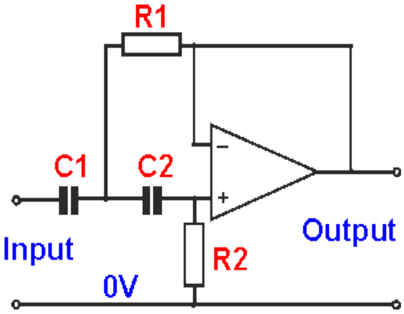
Single pole active high pass filter using an op amp
The cut off frequency or break point of the filter can be calculated very easily by working out the frequency at which the reactance of the capacitor equals the resistance of the resistor. This can be achieved using the formula:

$$X_c = \frac{1}{2 \pi f C}$$

Where:
Xc is the capacitive reactance in ohms
Π is equal to 3.142
f is the frequency in Hertz
C is the capacitance in Farads

Two pole active high pass filter

Although it is possible to design a wide variety of filters with different levels of gain and different roll off patterns using operational amplifiers, the filter described on this page will give a good sure-fire solution. It offers unity gain and a Butterworth response (the flattest response in band, but not the fastest to achieve ultimate roll off out of band).



Operational amplifier two pole high pass filter
Simple sure fire design with Butterworth response and unity gain
The calculations for the circuit values are very straightforward for the Butterworth response and unity gain scenario. Critical damping is required for the circuit and the ratio of the resistor vales determines this.

$$R1 = R2$$

$$C1 = 2 \times C2$$

$$f = \frac{\sqrt{2}}{4 \pi R \ C2}$$

When choosing the values, ensure that the resistor values fall in the region between 10 kΩ and 100 kΩ. This is advisable because the output impedance of the circuit rises with increasing frequency and values outside this region may affect the performance.

Successive Approximation type ADC

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.
(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

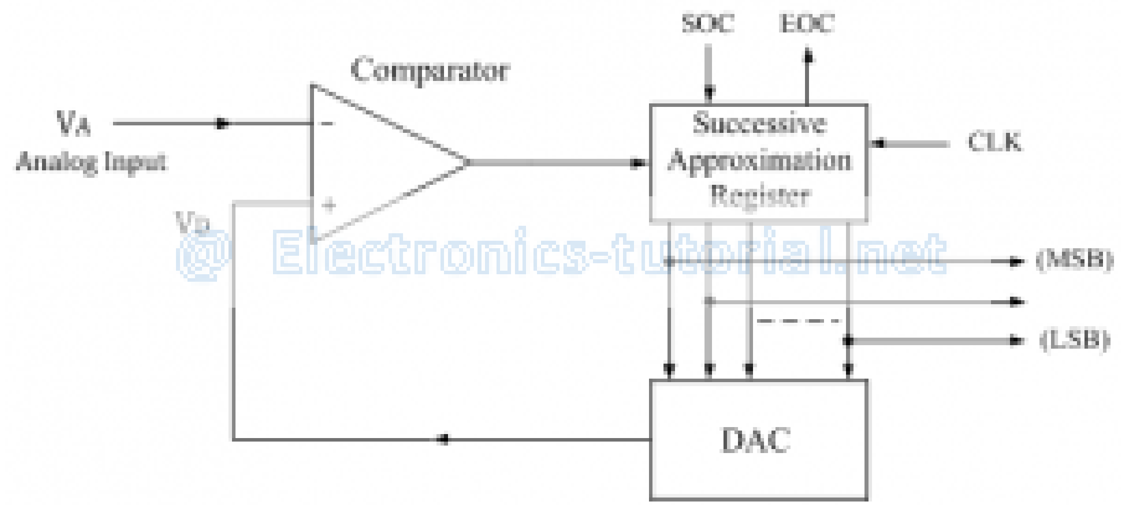
(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.
Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V. when the conversion starts, the MSB bit is set to 1.
Now VA = 11V > VD = 8V = [1000]2

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows
VD = 12V = [1100]2

Now VA = 11V < VD = 12V = [1100]2
Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as VD = 10V = [1010]2

Now again VA = 11V > VD = 10V = [1010]2
Again as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is
VD = 11V = [1011]2
Now finally VA = VD , and the conversion stops.
The functional block diagram of successive approximation type of ADC is shown below.

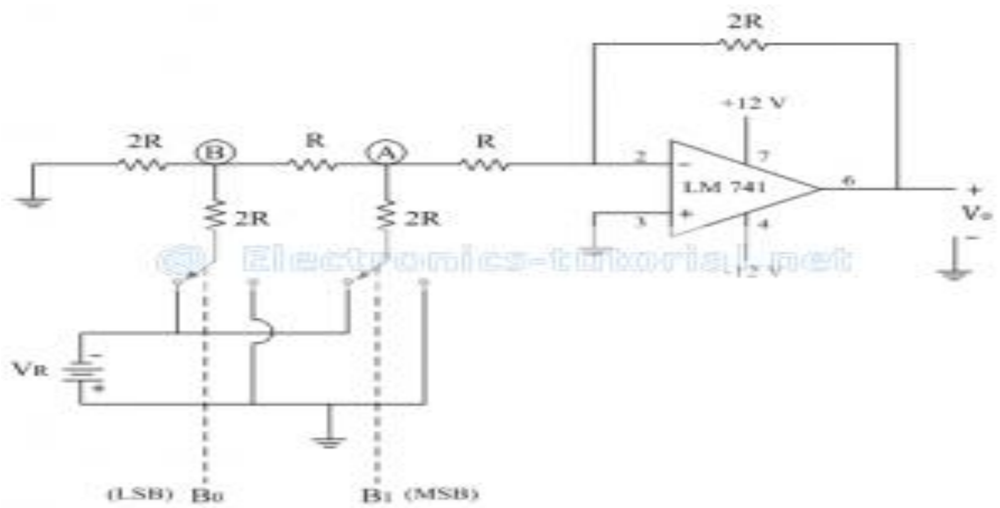


It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.
When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:
1 Conversion time is very small.
2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

R-2R LADDER DAC

The following circuit diagram shows the basic 2 bit R-2R ladder DAC circuit using op-amp. Here only two values of resistors are required i.e. R and 2R. The number of digits per binary word is assumed to be two (i.e. n = 2). The switch positions decides the binary word (i.e. B1 B0)



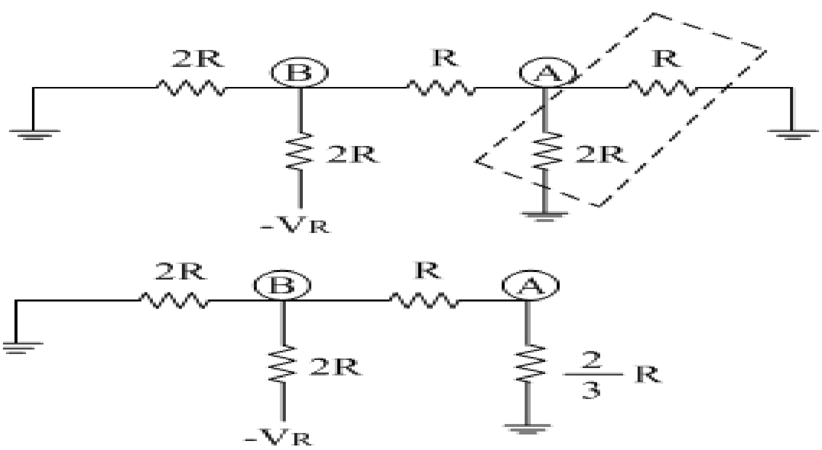
The typical value of feedback resistor is Rf = 2R. The resistance R is normally selected any value between 2.5 kΩ to 10 kΩ.
The generalized analog output voltage equation can be given as

$$V_o=-V_R\frac{R_f}{R}\left[\frac{B_1}{2^1}+\frac{B_2}{2^2}+\frac{B_3}{2^3}+----+\frac{B_n}{2^n}\right]$$

$$\therefore V_o=-V_R\frac{R_f}{R\times 2^n}[B_1 2^{n-1}+B_2 2^{n-2}+B_3 2^{n-3}+--+B_n 2^{n-n}]$$

$$\therefore V_o=-V_R\frac{R_f}{R\times 2^n}[B_1 2^{n-1}+B_2 2^{n-2}+B_3 2^{n-3}+--+B_n 2^0]$$

The operation of the above ladder type DAC is explained with the binary word (B1B0= 01)
The above circuit can be drawn as,



Applying the nodal analysis concept at point (A), we gets following equations

$$\frac{V_A}{\frac{2}{3}R} + \frac{V_A - V_B}{R} = 0$$

$$\therefore \frac{3V_A}{2R} + \frac{V_A - V_B}{R} = 0$$

$$\therefore \frac{3V_A + 2V_A - 2V_B}{2R} = 0$$

$$\therefore \; 5V_A = 2V_B$$

$$\therefore \; V_B = \frac{5V_A}{2}$$

Applying the nodal analysis concept at point (B), we gets following equations

$$\frac{V_B}{2R} + \frac{V_B - (-V_R)}{2R} + \frac{V_B - V_A}{R} = 0$$

$$\therefore \frac{V_B + V_B + V_R + 2V_B - 2V_A}{2R} = 0$$

$$\therefore \frac{4V_B + V_R - 2V_A}{2R} = 0$$

$$\therefore 4V_B + V_R - 2V_A = 0$$

$$\therefore V_A = 2V_B + V_R/2$$

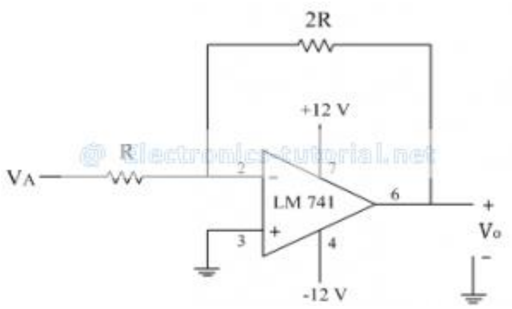
Substituting the equation of VB in the above equation, we get

$$\therefore V_A = 2\,\frac{5}{2}\,V_A + \frac{V_R}{2}$$

$$\therefore V_A = 5V_A + \frac{V_R}{4}$$

$$\therefore V_A = -\frac{V_R}{8}$$

The voltage at point A i.e. VA is applied as input to the op-amp which is in inverting amplifier mode as shown in figure below.



The output voltage of the complete setup

∴Vo= - (2R/R) VA

∴Vo= - (2R/R) (-VR/8)

∴Vo= VR/4

Similarly for other three combinations of digital input the analog output voltage Vo is calculated as follows

Sr. No.	Digital Input		Analog Output, $V_o(V)$
	B_1	B_0	
01	0	0	0
02	0	1	$\frac{V_R}{4}$
03	1	0	$\frac{2V_R}{4}$
04	1	1	$\frac{3V_R}{4}$

Successive Approximation type ADC

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digitaloutput, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.

Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V. when the conversion starts, the MSB bit is set to 1.

Now VA = 11V > VD = 8V = [1000]2

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows

VD = 12V = [1100]2

Now VA = 11V < VD = 12V = [1100]2

Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as

VD = 10V = [1010]2

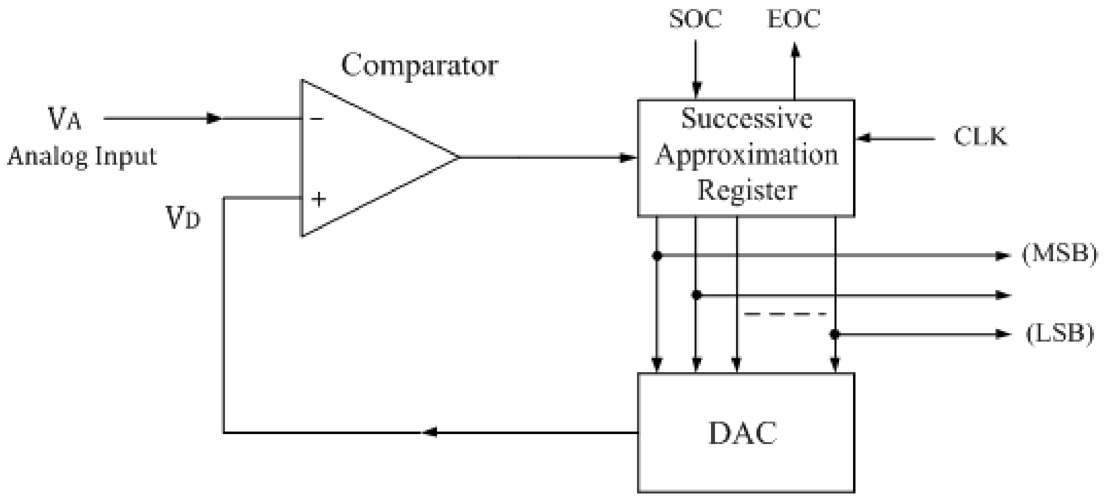
Now again VA = 11V > VD = 10V = [1010]2

Again as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is

VD = 11V = [1011]2

Now finally VA = VD , and the conversion stops.

The functional block diagram of successive approximation type of ADC is shown below.



It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.
When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:

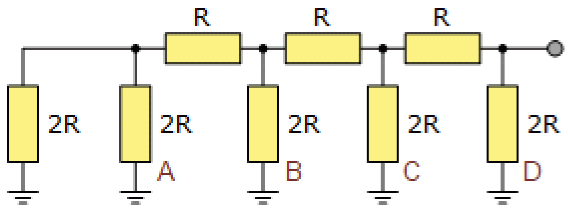
1 Conversion time is very small.

2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:

1 Circuit is complex.

2 The conversion time is more compared to flash type ADC.



R-2R DAC

R-2R Digital-to-Analogue Converter, or DAC, is a data converter which use two precision resistor to convert a digital binary number into an analogue output signal proportional to the value of the digital number

We saw in the previous tutorial about the **binary weighted digital-to-analogue converter** that the analogue output voltage is the weighted sum of the individual inputs, and that it requires a large range of precision resistors within its ladder network, making its design both expensive and impractical for most DAC's requiring lower levels of resolution.

We also saw that the binary weighted DAC is based on a closed-loop inverting operational amplifier using summing amplifier topology. While this type of data converter configuration works well for a D/A converter of a few bits of resolution, a much simpler approach is to use a R-2R resistive ladder network to construct a **R-2R Digital-to-Analogue Converter** which requires only two precision resistances.

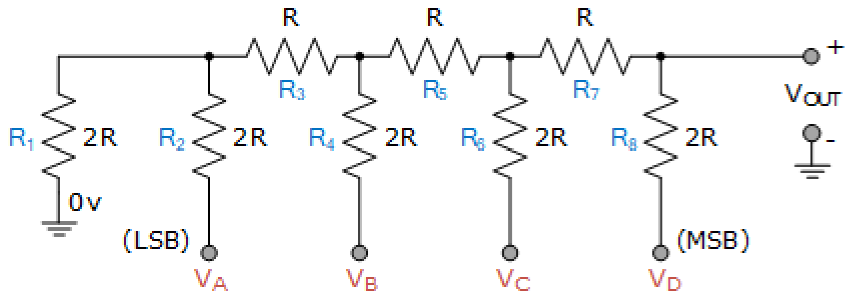
The R-2R resistive ladder network uses just two resistor values, one which is the base value "R" and the other which has twice the value, "2R" of the first resistor no matter how many bits are used to make up the ladder network. So for example, we could just use a 1kΩ resistor for the base resistor "R", and therefore a 2kΩ resistor for "2R" (or multiples thereof as the base value of R is not too critical), thus 2R is always twice the value of R, that is 2R = 2*R. This means that it is much easier to maintain the required accuracy of the resistors along the ladder network compared to the previous weighted resistor DAC. But what is a "R-2R resistive ladder network" anyway.

R-2R Resistive Ladder Network

As its name implies, the "ladder" description comes from the ladder-like configuration of the resistors used within the network. A R-2R resistive ladder network provides a simple means of converting digital voltage signals into an equivalent analogue output. Input voltages are applied to the ladder network at various points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier.

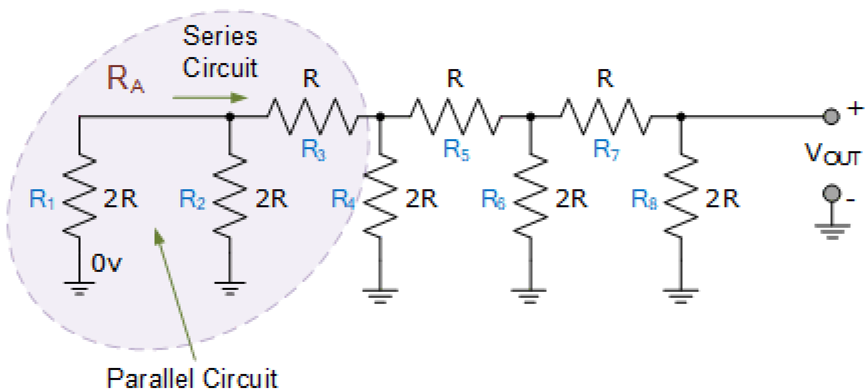
Then a R-2R resistive ladder network is nothing more than long strings of parallel and series connected resistors acting as interconnected voltage dividers along its length, and whose output voltage depends soley on the interaction of the input voltages with each other. Consider the basic 4-bit R-2R ladder network (4-bits because it has four input points) below.

4-bit R-2R Resistive Ladder Network



This 4-bit resistive ladder circuit may look complicated, but its all about connecting resistors together in parallel and series combinations and working back to the input source using simple circuit laws to find the proportional value of the output. Lets assume all the binary inputs are grounded at 0 volts, that is: $V_A = V_B = V_C = V_D = 0V$ (LOW). The binary code corresponding to these four inputs will therefore be: **0000**.

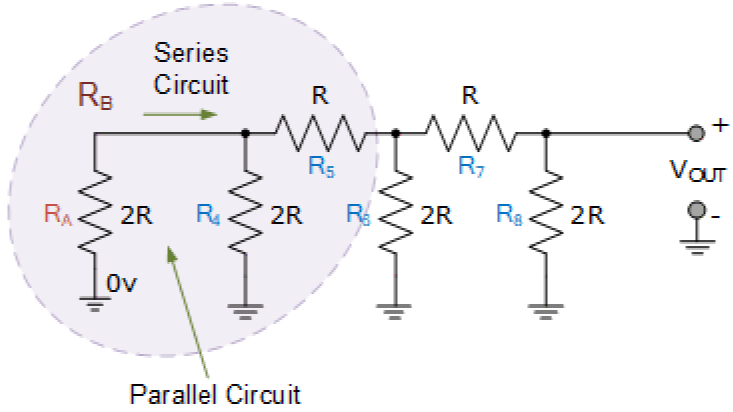
Starting from the left hand side and using the simplified equation for two parallel resistors and series resistors, we can find the equivalent resistance of the ladder network as:



Resistors R_1 and R_2 are in "parallel" with each other but in "series" with resistor R_3. Then we can find the equivalent resistance of these three resistors and call it R_A for simplicity (or any other form of identification you want).

$$R_A = R_3 + \frac{R_1 \times R_2}{R_1 + R_2} = R + \frac{2R \times 2R}{2R + 2R} = R + R = 2R$$

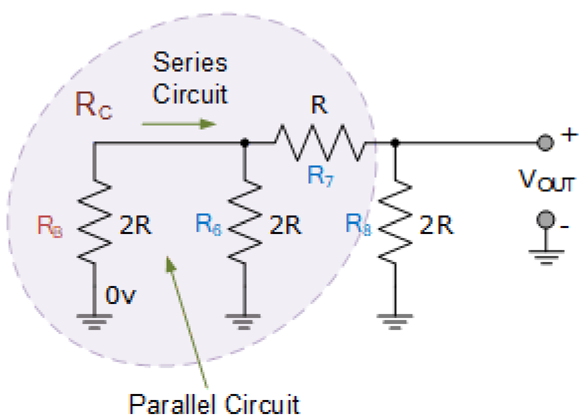
Then R_A is equivalent to "2R". Now we can see that the equivalent resistance "R_A" is in parallel with R_4 with the parallel combination in series with R_5.



Again we can find the equivalent resistance of this combination and call it R_B.

$$R_B = R_5 + \frac{R_A \times R_4}{R_A + R_4} = R + \frac{2R \times 2R}{2R + 2R} = R + R = 2R$$

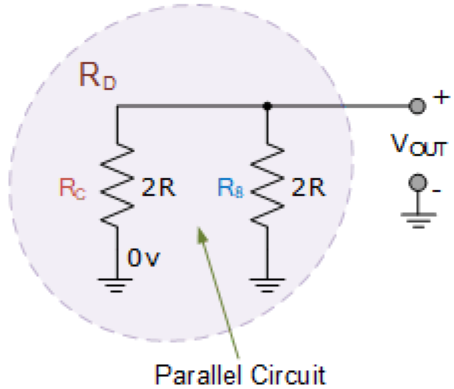
So R_B combination is equivalent to "2R". Hopefully we can see that this equivalent resistance R_B is in parallel with R_6 with the parallel combination in series with R_7 as shown.



As before we find the equivalent resistance and call it R_C.

$$R_C = R_7 + \frac{R_B \times R_6}{R_B + R_6} = R + \frac{2R \times 2R}{2R + 2R} = R + R = 2R$$

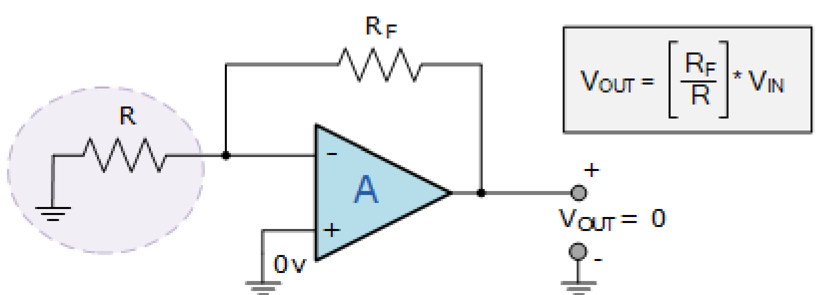
Again, resistor combination R_C is equivalent to "2R" which is in parallel with R_8 as shown.



As we have shown above, when two equal resistor values are paralled together, the resulting value is one-half, so 2R in parallel with 2R equals an equivalent resistance of R. So the whole 4-bit R-2R resistive ladder network comprising of individual resistors connected together in parallel and series combinations has an equivalent resistance (R_{EQ}) of "R" when a binary code of "0000" is applied to its four inputs.

Therefore with a binary code of "0000" applied as inputs, our basic 4-bit R-2R digital-to-analogue converter circuit would look something like this:

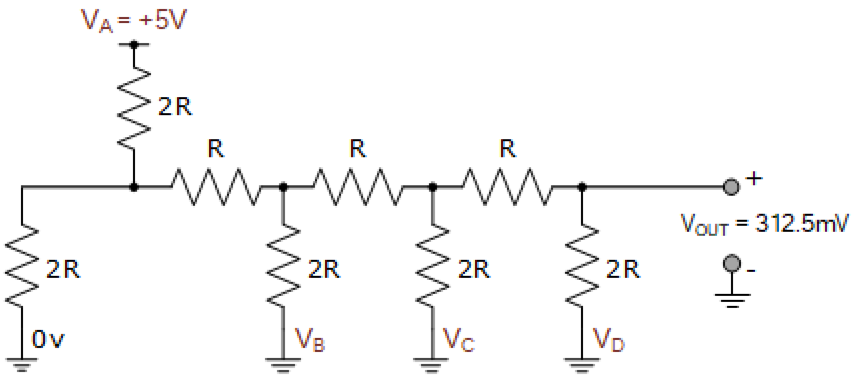
R-2R DAC Circuit with Four Zero (LOW) Inputs



The ouput voltage for an inverting operational amplifier is given as: $(R_F/R_{IN})*V_{IN}$. If we make R_F equal to R, that is R_F = R = 1, and as R is terminated to ground (0V), then there is no V_{IN} voltage value, (V_{IN} = 0) so the output voltage would be: (1/1)*0 = 0 volts. So for a 4-bit R-2R DAC with four grounded inputs (LOW), the output voltage will be "zero" volts, thus a 4-bit digital input of **0000** produces an analogue output of 0 volts.

So what happens now if we connect input bit V_A HIGH to +5 volts. What would be the equivalent resistive value of the R-2R ladder network and the output voltage from the op-amp.

R-2R DAC with Input V_A

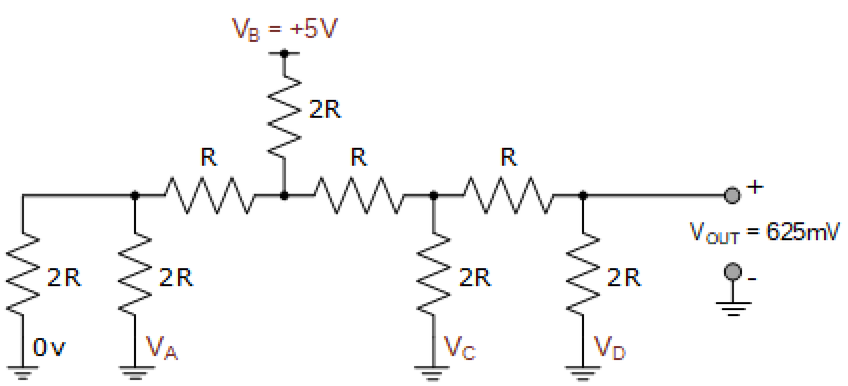


Input V_A is HIGH and logic level "1" and all the other inputs grounded at logic level "0". As the R/2R ladder network is a linear circuit we can find Thevenin's equivalent resistance using the same parallel and series resistance calculations as above to calculate the expected output voltage. The output voltage, V_{OUT} is therefore calculated at 312.5 milli-volts (312.5 mV).

As we have a 4-bit R-2R resistive ladder network, this 312.5 mV voltage change is one-sixteenth the value of the +5V input (5/0.3125 = 16) voltage so is classed as the Least Significant Bit, (LSB). Being the least significant bit, input V_A will therefore determine the "resolution" of our simple 4-bit digital-to-analogue converter, as the smallest voltage change in the analogue output corresponds to a single step change of the digital inputs. Thus for our 4-bit DAC this will be 312.5mV (1/16th) for a +5V input.

Now lets see what happens to the output voltage if we connect input bit V_B HIGH to +5 volts.

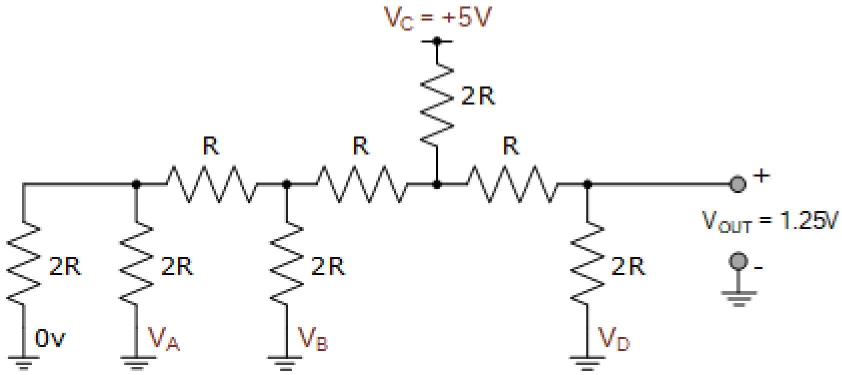
R-2R DAC with Input V_B



With input V_B HIGH and logic level "1" and all the other inputs grounded at logic level "0", the output voltage, V_{OUT} is calculated at 625mV, and which is one-eighth (1/8th) the value of the +5V input (5/0.625 = 8) voltage. We can also see that it is double the output voltage when only input bit V_A was applied, and we would expect this as its the 2_{nd} bit (input) so has double the weighting of the 1_{st} bit.

Now lets see what happens to the output voltage if we connect input bit V_C HIGH to +5 volts.

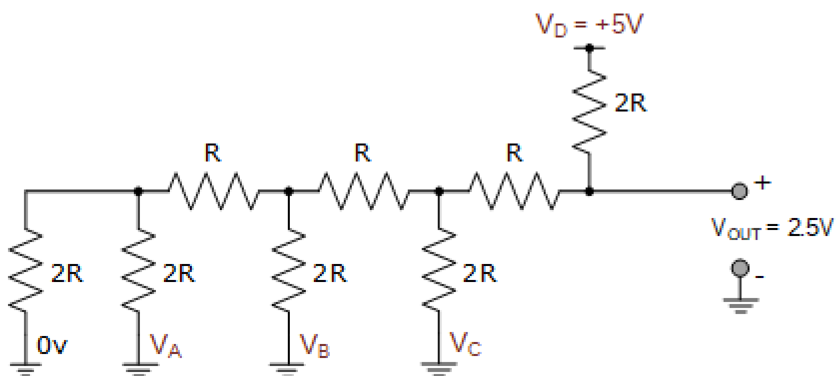
R-2R DAC with Input V_C



With input V_C HIGH and logic level "1" and the other input bits at logic level "0", the output voltage, V_{OUT} is calculated at 1.25 volts, and which is one-quarter (1/4) the value of the +5V input (5/1.25 = 4) voltage. Again we can see that this voltage is double the output of input bit V_B but also 4 times the value of bit V_A. This is because input V_C is the 3_{rd} bit so has double the weighting of the 2_{nd} bit and four times the weighting of the 1_{st} bit.

Finally lets see what happens to the output voltage if we connect input V_D HIGH to +5 volts.

R-2R DAC with Input V_D



With only input V_D HIGH and logic level "1" and the other inputs at logic level "0", the output voltage, V_{OUT} is calculated at 2.5 volts. This is on-half (1/2) the value of the +5V input (5/2.5 = 2) voltage. Again we can see that this voltage is double the output of input bit V_C, 4 times the value of bit V_B and 8 times the value of input bit V_A as it is the 4_{th} bit and therefore classed as the Most Significant Bit, (MSB).

Then we can see that if input V_A represents the LSB and therefore controls the DAC's resolution, and input V_B is double V_A, input V_C is four times greater than V_A, and input V_D is eight times greater than V_A, we can obtain a relationship for the analogue output voltage of our 4-bit digital-to-analogue converter with the following equation:

Digital-to-Analogue Output Voltage Equation

$$V_{OUT} = \frac{V_A + 2V_B + 4V_C + 8V_D}{16}$$

Where the denominator value of 16 corresponds to the 16 (2^4) possible combinations of inputs to the 4-bit R-2R ladder network of the DAC.

We can expand this equation further to obtain a generalised R-2R DAC equation for any number of digital inputs for a R-2R D/A converter as the weighting of each input bit will always be referenced to the least significant bit (LSB), giving us a generalised equation of:

Generalised R-2R DAC Equation

$$V_{OUT} = \frac{V_A + 2V_B + 4V_C + 8V_D + 16V_E + 32V_F + \ldots etc}{2^n}$$

Where: "n" represents the number of digital inputs within the R-2R resistive ladder network of the DAC producing a resolution of: $V_{LSB} = V_{IN}/2^n$.

Clearly then input bit V_A when HIGH will cause the smallest change in the output voltage, while input bit V_D when HIGH will cause the greatest change in the output voltage. The expected output voltage is therefore calculated by summing the effect of all the individual input bits which are connected HIGH.

Ideally, the ladder network should produce a linear relationship between the input voltages and the analogue output as each input will have a step increase equal to the LSB, we can create a table of expected output voltage values for all 16 combinations of the 4 inputs with +5V representing a logic "1" condition as shown.

4-bit R-2R D/A Converter Output

Digital Inputs				V_{OUT} Expression	V_{OUT}
D	C	B	A	$(8*V_D + 4*V_C + 2*V_B + 1*V_A)/2^4$	in Volts
0	0	0	0	(0*5 + 0*5 + 0*5 + 0*5)/16	0
0	0	0	1	(0*5 + 0*5 + 0*5 + 1*5)/16	0.3125
0	0	1	0	(0*5 + 0*5 + 2*5 + 0*5)/16	0.6250
0	0	1	1	(0*5 + 0*5 + 2*5 + 1*5)/16	0.9375

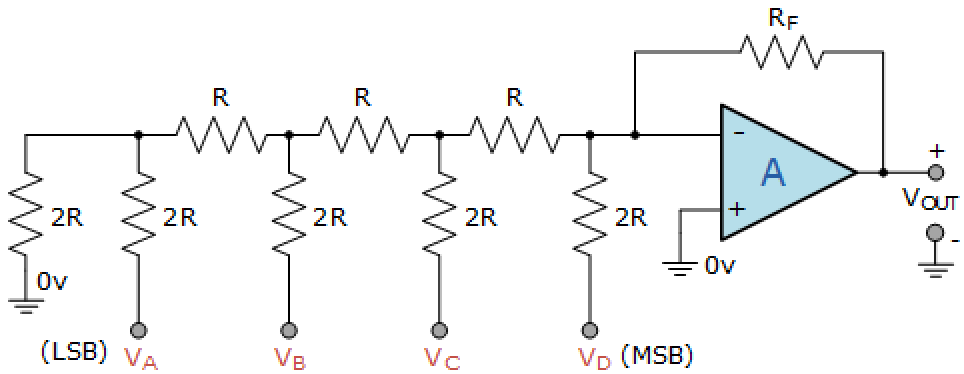
0	1	0	0	(0*5 + 4*5 + 0*5 + 0*5)/16	1.2500
0	1	0	1	(0*5 + 4*5 + 0*5 + 1*5)/16	1.5625
0	1	1	0	(0*5 + 4*5 + 2*5 + 0*5)/16	1.8750
0	1	1	1	(0*5 + 4*5 + 2*5 + 1*5)/16	2.1875
1	0	0	0	(8*5 + 0*5 + 0*5 + 0*5)/16	2.5000
1	0	0	1	(8*5 + 0*5 + 0*5 + 1*5)/16	2.8125
1	0	1	0	(8*5 + 0*5 + 2*5 + 0*5)/16	3.1250
1	0	1	1	(8*5 + 0*5 + 2*5 + 1*5)/16	3.4375
1	1	0	0	(8*5 + 4*5 + 0*5 + 0*5)/16	3.7500
1	1	0	1	(8*5 + 4*5 + 0*5 + 1*5)/16	4.0625
1	1	1	0	(8*5 + 4*5 + 2*5 + 0*5)/16	4.3750
1	1	1	1	(8*5 + 4*5 + 2*5 + 1*5)/16	4.6875

Notice that the full-scale analogue output voltage for a binary code of **1111** never reaches the same value as the digital input voltage (+5V) but is less by the equivalent of one LSB bit, (312.5mV in this example). However, the higher the number of digital input bits (resolution) the nearer the analogue output voltage reaches full-scale when all the input bits are HIGH. Likewise when all the input bits are LOW, the resulting lower resolution of LSB makes V_{OUT} closer to zero volts.

R-2R Digital-to-Analogue Converter

Now that we understand what a *R-2R resistive ladder network* is and how it works, we can use it to produce a R-2R Digital-to-Analogue Converter. Again using our 4-bit R-2R resistive ladder network from above and adding it to an inverting operational amplifier circuit, we can create a simple R-2R digital-to-analogue converter of:

R-2R Digital-to-Analogue Converter



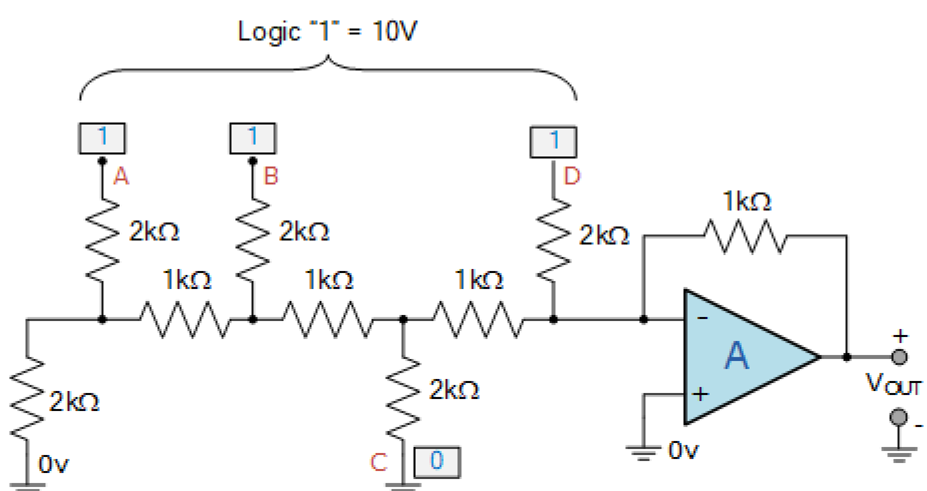
The digital logic circuit used to drive the D/A converter can be generated by combinational or sequential logic circuits, data registers, counters or simply switches. The interfacing of a R-2R D/A converter of "n"-bits will depend upon its application. All-in-one boards such as the Arduino or Raspberry Pi have *digital-to-analogue converters* built-in so make interfacing and programming much easier. There are many popular DAC's available such as the 8-bit DAC0808.

R-2R D/A Converter Example No1

A 4-bit R-2R digital-to-analogue converter is constructed to control the speed of a small DC motor using the output from a digital logic circuit. If the logic circuit uses 10 volt CMOS devices, calculate the analogue output voltage from the DAC when the input code is hexadecimal number "B". Also determine the resolution of the DAC.

1). The hexadecimal letter "B" is equal to the number eleven in decimal. The decimal number eleven is equal to the binary code "1011" in binary. That is: $B_{16} = 1011_2$. Thus for our 4-bit binary number of 1011_2, input bit D = 1, bit C = 0, bit B = 1 and bit A = 1.

If we assume that feedback resistor R_F is equal to "R", then our R-2R D/A converter circuit will look like:



The digital logic circuit uses 10 volt CMOS devices, so the input voltage to the R-2R network will be 10 volts. Also being a 4-bit ladder DAC, there will be 2^4 possible input combinations, so using our equation from above, the ouput voltage for a binary code of 1011_2 is calculated as:

$$V_{OUT} = \frac{1V_A + 2V_B + 4V_C + 8V_D}{2^n}$$

$$V_{OUT} = \frac{1\times10 + 2\times10 + 4\times0 + 8\times10}{16}$$

$$V_{OUT} = \frac{110}{16} = 6.875 \text{ Volts}$$

Therefore the analogue output voltage used to control the DC motor when the input code is 1011_2 is calculated as: -6.875 volts. Note that the output voltage is negative due to the inverting input of the operational amplifier.

2). The resolution of the converter will be equal to the value of the least significant bit (LSB) which is given as:

$$\text{Resolution} = V_{(LSB)} = \frac{V_{IN}}{2^n}$$

$$\therefore \text{ Resolution} = \frac{10}{16} = 0.625 \text{ Volts}$$

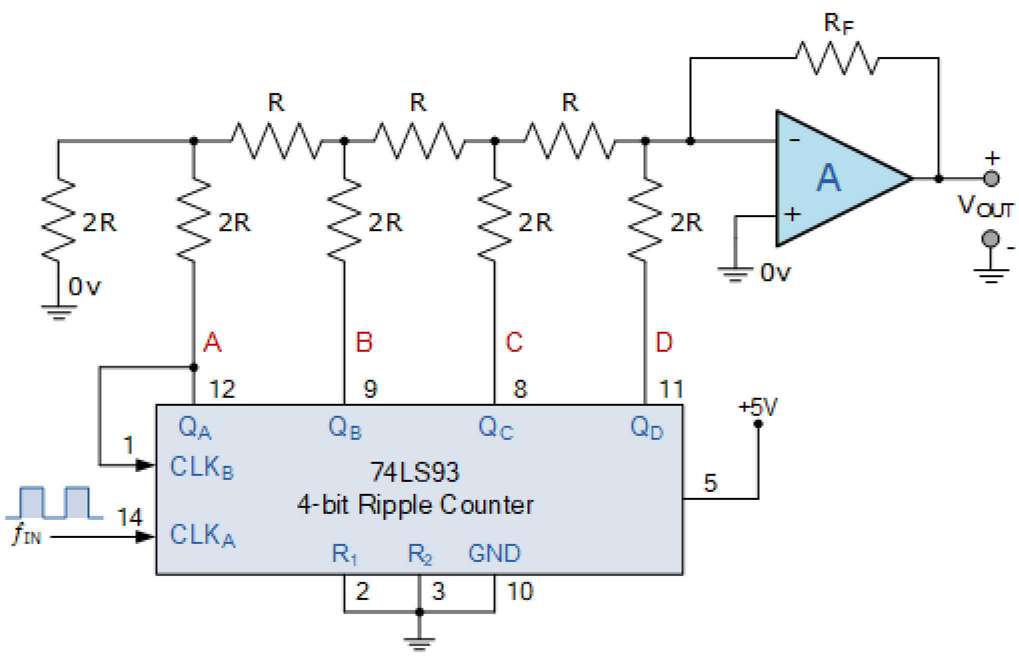
Then the smallest step change of the analogue output voltage, V_{OUT} for a 1-bit LSB change of the digital input of this 4-bit R-2R digital-to-analogue converter example is: 0.625 volts. That is the output voltage changes in steps or increments of 0.625 volts and not as a straight linear value.

4-bit Binary Counting R-2R DAC

Hopefully by now we understand that we can make a R-2R ladder DAC using just two resistor values, one the base value "R" and the other twice or double the value being "2R". In our simple example above we have made a 4-bit R-2R DAC with four input data lines, A, B, C, and D giving us 16 (2^4) different input combinations from "0000" to "1111". The binary code for these four digital input lines can be generated in many different ways, using micro-controllers, digital circuits, mechanical or solid state switches. But one interesting option is to use a 4-bit binary counter such as the 74LS93.

The **74LS93** is a 4-bit J-K ripple counter which can be configured to count-up from 0000_2 to 1111_2 (MOD-16) and reset back to zero (0000) again by the application of a single external clock signal. The 74LS93 is an asynchronous counter commonly called a "ripple" counter because of the way that the internal J-K bistables respond to the clock or timing input producing a 4-bit binary output. The frequency (or period) of this external clock or timing pulse is divided by a factor of 2, 4, 8, and 16 by the counters output lines as the clock pulse appears to ripple through the four J-K flip-flops producing the required 4-bit output count sequence from 0000_2 to 1111_2.

4-bit Binary Counting R-2R DAC



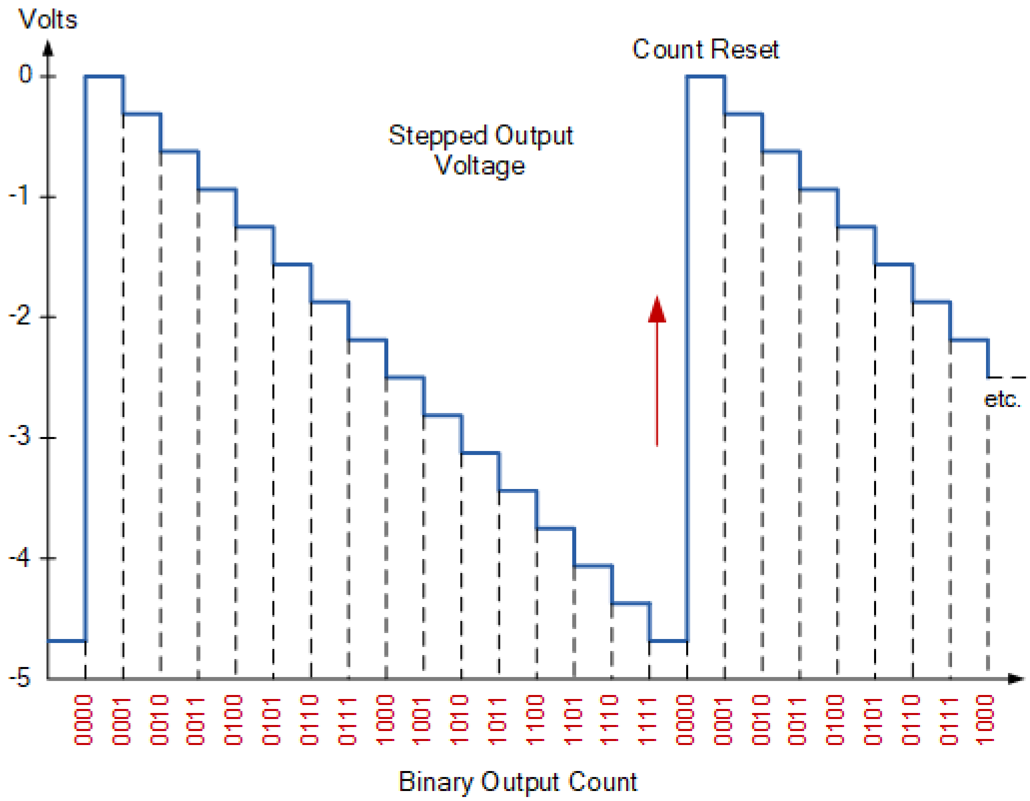
Note that to count upwards from 0000 to 1111, the external CLK_B input must be connected to the Q_A (pin-12) output and the input timing pulses are applied to input CLK_A (pin-14).

This simple 4-bit asynchronous up counter built around the 74LS93 binary ripple counter as the same counting sequence given in the above table. On the application of a clock pulse the outputs: Q_A, Q_B, Q_C, and Q_D change by one step. The input of the operational amplifier detects this step change and outputs a negative voltage (inverting op-amp) relative to the binary code at the R-2R ladder inputs. The output voltage value for each step will correspond to that given in the table above.

The ripple counter will count up in sequence with the four outputs producing an output sequence of binary values upto the 15th clock pulse where the outputs are set to 1111_2 (decimal 15) producing the maximum negative output voltage of the digital-to-analogue converter. On the 16th pulse the counters output sequence is reset and the count returns back to 0000, which resets the op-amps output back to zero volts. The application of the next clock pulse begins a new counting cycle from zero to $V_{OUT(max)}$.

We can show the output sequence for this simple 4-bit binary asynchronous counting R-2R D/A converter in the following timing diagram.

4-bit R-2R DAC Timing Diagram



Clearly then, the output voltage of the operational amplifier varies from zero volts to its maximum negative voltage as the ripple counter counts from 0000_2 to 1111_2 respectively. This simple circuit could be used to vary the brightness of a lamp connected to the op-amps output, or continually vary the speed of a DC motor from slow to fast, and back to slow again at a rate determined by the clock period.

Here the ripple counter and R-2R DAC are configured for 4-bit operation but using commonly available binary ripple counters such as the CMOS 4024 7-bit (÷128), the CMOS 4040 12-bit (÷4096) or the larger CMOS 4060 14-bit (÷16,384) counter and adding more input resistors to the R-2R ladder network such as those available from **Bournes**, the resolution (LSB) of the circuit can be greatly lowered producing a smoother output signal from the *R-2R digital-to-analogue converter*.

2 Comments

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Ganesh Jambhale

For R-2R network, What is the input for each input?

Posted on May 25th 2021 | 8:54 am

Reply

Douglas Goldfarb

I think circuit. Designs were very Interesting

Posted on February 19th 2021 | 3:42 pm

Reply
