CHAPTER

5

The Field-Effect Transistor

5.0 PREVIEW

In the last two chapters, we looked at the bipolar junction transistor and BJT circuits. In this chapter, we introduce the second major type of transistor, the field-effect transistor (FET). There are two general classes of FETs: the metal-oxide-semiconductor FET (MOSFET) and the junction FET (JFET). The MOSFET has led to the second electronics revolution in the 1970s and 1980s, in which the microprocessor has made possible powerful desktop computers and sophisticated hand-held calculators. The MOSFET can be made very small, so high-density VLSI circuits and high-density memories are possible.

We begin the chapter with a look at the physical structure and operation of the MOSFET. The current–voltage characteristics of the device are developed, and then the dc analysis and design of MOSFET circuits are considered. We will see how the MOSFET can be used in place of resistors in a circuit, so that circuits containing only MOSFETs can be designed.

In the junction FET, the junction may be a pn junction, which forms a pn JFET, or a Schottky barrier junction, which forms a metal-semiconductor FET, or MESFET. MESFETs are used in very high speed or high-frequency applications, such as microwave amplifiers. Since JFETs are specialized devices, the discussion of JFET circuits is brief.

Although the emphasis of this chapter is on dc circuits, we discuss how the FET can be used in switch, digital, and linear amplifier applications. A major goal of this chapter is to enable the reader to become very familiar and comfortable with the MOSFET properties and to be able to quickly analyze and design the dc response of FET circuits.

5.1 MOS FIELD-EFFECT TRANSISTOR

The **metal-oxide-semiconductor field-effect transistor (MOSFET)** became a practical reality in the 1970s. The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC chip). Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high-density VLSI circuits, including microprocessors and memories, can be fabricated. The MOSFET has made possible the hand-held calculator and

the powerful personal computer. MOSFETs can also be used in analog circuits, as we will see in the next chapter.

In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the **field effect**. Again, the basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

In the following two sections, we will discuss the various types of MOSFETs, develop the *i*–*v* characteristics, and then consider the dc biasing of various MOSFET circuit configurations. After studying these sections, you should be familiar and comfortable with the MOSFET and MOSFET circuits.

5.1.1 Two-Terminal MOS Structure

The heart of the MOSFET is the metal-oxide-semiconductor capacitor shown in Figure 5.1. The metal may be aluminum or some other type of metal. In many cases, the metal is replaced by a high-conductivity polycrystalline silicon layer deposited on the oxide. However, the term metal is usually still used in referring to MOSFETs. In the figure, the parameter t_{ox} is the thickness of the oxide and ϵ_{ox} is the oxide permittivity.

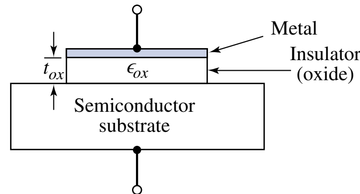


Figure 5.1 The basic MOS capacitor structure

The physics of the MOS structure can be explained with the aid of a simple parallel-plate capacitor.[1] Figure 5.2(a) shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates, as shown.

A MOS capacitor with a p-type semiconductor substrate is shown in Figure 5.2(b). The top metal terminal, also called the **gate**, is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced in the direction shown in the figure. If the electric field penetrates the semiconductor, the holes in the p-type semiconductor will experience a force toward the oxide-semiconductor inter-

[1]The capacitance of a parallel plate capacitor, neglecting fringing fields, is $C = \epsilon A/d$, where A is the area of one plate, d is the distance between plates, and ϵ is the permittivity of the medium between the plates.

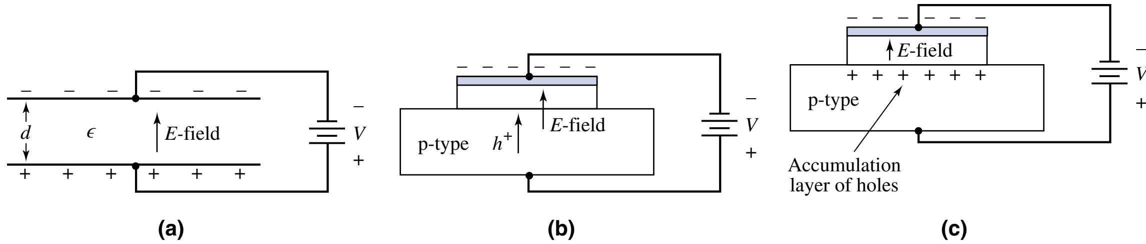


Figure 5.2 (a) A parallel-plate capacitor, showing the electric field and conductor charges, (b) a corresponding MOS capacitor with a negative gate bias, showing the electric field and charge flow, and (c) the MOS capacitor with an accumulation layer of holes

face. The equilibrium distribution of charge in the MOS capacitor with this particular applied voltage is shown in Figure 5.2(c). An accumulation layer of positively-charged holes in the oxide-semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

Figure 5.3(a) shows the same MOS capacitor, but with the polarity of the applied voltage reversed. A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction, as shown. In this case, if the electric field penetrates the semiconductor, holes in the p-type material will experience a force away from the oxide-semiconductor interface. As the holes are pushed away from the interface, a negative space-charge region is created, due to the fixed acceptor impurity atoms. The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor. Figure 5.3(b) shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage.

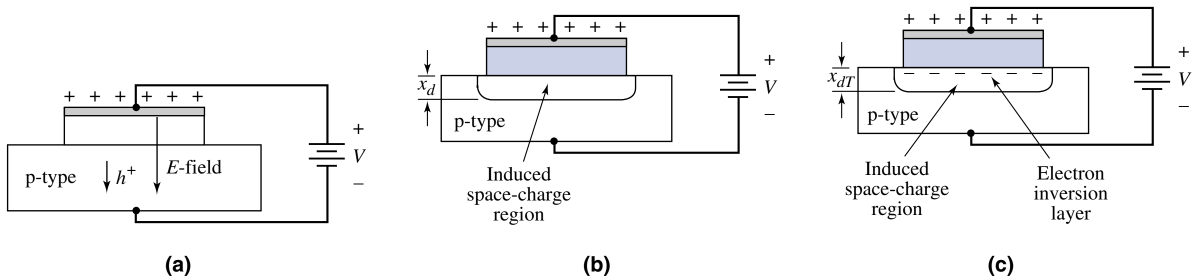


Figure 5.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate gate bias, and (c) the MOS capacitor with an induced space-charge region and electron inversion layer due to a larger gate bias

When a larger positive voltage is applied to the gate, the magnitude of the induced electric field increases. Minority carrier electrons are attracted to the oxide-semiconductor interface, as shown in Figure 5.3(c). This region of minority carrier electrons is called an **electron inversion layer**. The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

The same basic charge distributions can be obtained in a MOS capacitor with an n-type semiconductor substrate. Figure 5.4(a) shows this MOS capacitor structure, with a positive voltage applied to the top gate terminal. A positive charge is created on the top gate and an electric field is induced in the

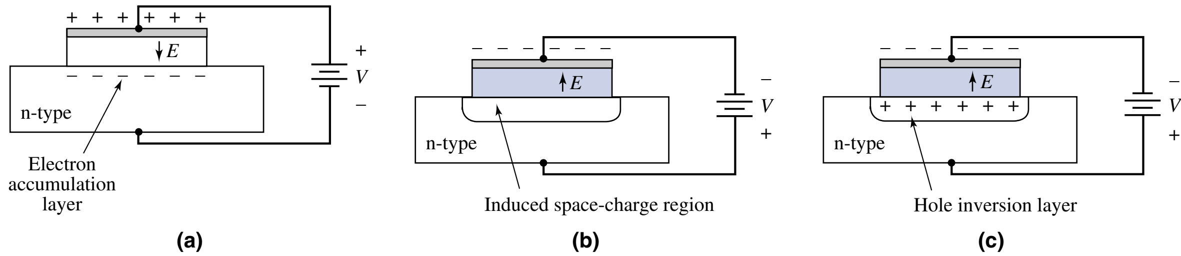


Figure 5.4 The MOS capacitor with n-type substrate for: (a) a positive gate bias, (b) a moderate negative bias, and (c) a larger negative bias

direction shown. In this situation, an accumulation layer of electrons is induced in the n-type semiconductor.

Figure 5.4(b) shows the case when a negative voltage is applied to the gate terminal. A positive space-charge region is induced in the n-type substrate by the induced electric field. When a larger negative voltage is applied, a region of positive charge is created at the oxide-semiconductor interface, as shown in Figure 5.4(c). This region of minority carrier holes is called a **hole inversion layer**. The magnitude of the positive charge in the inversion layer is a function of the applied gate voltage.

The term **enhancement mode** means that a voltage must be applied to the gate to create an inversion layer. For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

5.1.2 n-Channel Enhancement-Mode MOSFET

We will now apply the concepts of an inversion layer charge in a MOS capacitor to create a transistor.

Transistor Structure

Figure 5.5(a) shows a simplified cross section of a MOS field-effect transistor. The gate, oxide, and p-type substrate regions are the same as those of a MOS capacitor. In addition, we now have two n-regions, called the **source terminal** and **drain terminal**. The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the **channel region**, adjacent to the oxide–semiconductor interface.

The channel length L and channel width W are defined on the figure. The channel length of a typical integrated circuit MOSFET is less than 1 μm (10^{-6} m), which means that MOSFETs are small devices. The oxide thickness t_{ox} is typically on the order of 400 angstroms, or less.

The diagram in Figure 5.5(a) is a simplified sketch of the basic structure of the transistor. Figure 5.5(b) shows a more detailed cross section of a MOSFET fabricated into an integrated circuit configuration. A thick oxide, called the **field oxide**, is deposited outside the area in which the metal interconnect lines are formed. The gate material is usually heavily doped polysilicon. Even though the actual structure of a MOSFET may be fairly complex, the simplified diagram may be used to develop the basic transistor characteristics.

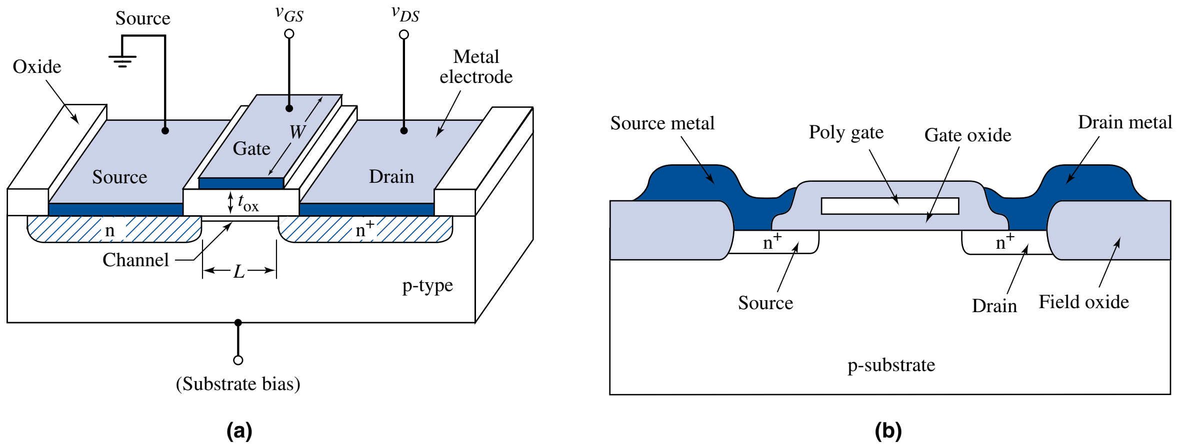


Figure 5.5 (a) Schematic diagram of an n-channel enhancement mode MOSFET and (b) an n-channel MOSFET, showing the field oxide and polysilicon gate

Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 5.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 5.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer "connects" the n-source to the n-drain, as shown in Figure 5.6(c). A current can then be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement-mode MOSFET**. Also, since the carriers in the inversion layer are electrons, this device is also called an **n-channel MOSFET**.

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, or **NMOS transistor**, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional

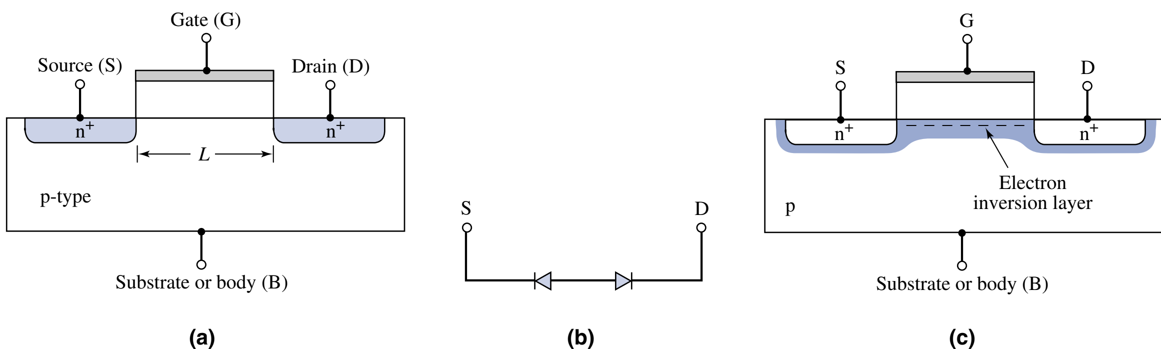


Figure 5.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

5.1.3 Ideal MOSFET Current–Voltage Characteristics

The **threshold voltage** of the n-channel MOSFET is denoted as V_{TN} and is defined[2] as the applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate. In simple terms, we can think of the threshold voltage as the gate voltage required to ‘‘turn on’’ the transistor.

For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge. If the gate voltage is less than the threshold voltage, the current in the device is essentially zero. If the gate voltage is greater than the threshold voltage, a drain-to-source current is generated as the drain-to-source voltage is applied. The gate and drain voltages are measured with respect to the source.

Figure 5.7(a) shows an n-channel enhancement-mode MOSFET with the source and substrate terminals connected to ground. The gate-to-source voltage is less than the threshhold voltage, and there is a small drain-to-source voltage. With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero (neglecting pn junction leakage currents).

Figure 5.7(b) shows the same MOSFET with an applied gate voltage greater than the threshold voltage. In this situation, an electron inversion layer is created and, when a small drain voltage is applied, electrons in the inversion layer flow from the source to the positive drain terminal. The conven-

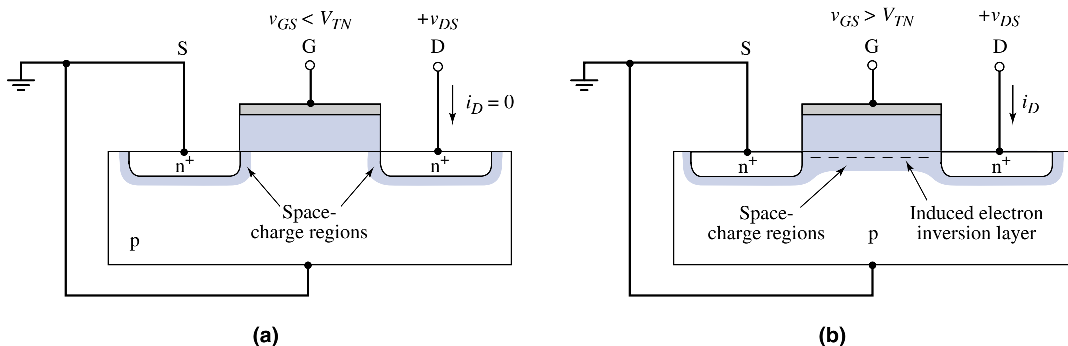


Figure 5.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

[2]The usual notation for threshold voltage is V_T. However, since we have defined the thermal voltage as $V_T = kT/q$, we will use V_{TN} for the threshold voltage of the n-channel device.

tional current enters the drain terminal and leaves the source terminal. Note that a positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.

The i_D versus v_{DS} characteristics for small values of v_{DS} are shown in Figure 5.8. When $v_{DS} < V_{TN}$, the drain current is zero. When v_{GS} is greater than V_{TN}, the channel inversion charge is formed and the drain current increases with v_{DS}. Then, with a larger gate voltage, a larger inversion charge density is created, and the drain current is greater for a given value of v_{DS}.

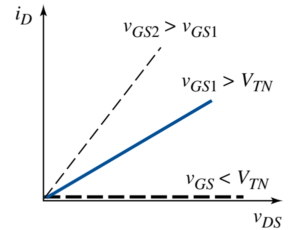


Figure 5.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

Figure 5.9(a) shows the basic MOS structure for $v_{GS} > V_{TN}$ and a small applied v_{DS}. In the figure, the thickness of the inversion channel layer qualitatively indicates the relative charge density, which for this case is essentially constant along the entire channel length. The corresponding i_D versus v_{DS} curve is also shown in the figure.

Figure 5.9(b) shows the situation when v_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the i_D versus v_{DS} curve to decrease. This effect is shown in the i_D versus v_{DS} curve in the figure.

As v_{DS} increases to the point where the potential difference across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density at the drain terminal is zero. This effect is shown schematically in Figure 5.9(c). For this condition, the incremental channel conductance at the drain is zero, which means that the slope of the i_D versus v_{DS} curve is zero. We can write

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN} \tag{5.1(a)}$$

or

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN} \tag{5.1(b)}$$

where $v_{DS}(\text{sat})$ is the drain-to-source voltage that produces zero inversion charge density at the drain terminal.

When v_{DS} becomes larger than $v_{DS}(\text{sat})$, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, are injected into the space-charge region, where they are swept by the E-field to the drain contact. This process is similar to electrons being swept across a reverse-biased B–C junction in a bipolar transistor. In the ideal MOSFET, the drain current is constant for $v_{DS} > v_{DS}(\text{sat})$. This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region**,[3] which is shown in Figure 5.9(d).

[3]The term saturation for MOSFETs is not to be confused with saturation for BJTs. We commonly say that a BJT is driven into *saturation*, which means that the collector current no longer increases with increasing base current and the collector–emitter voltage has reached a minimum value. When a MOSFET is biased in the *saturation region*, the drain current is essentially independent of drain voltage for a constant gate-to-source voltage.

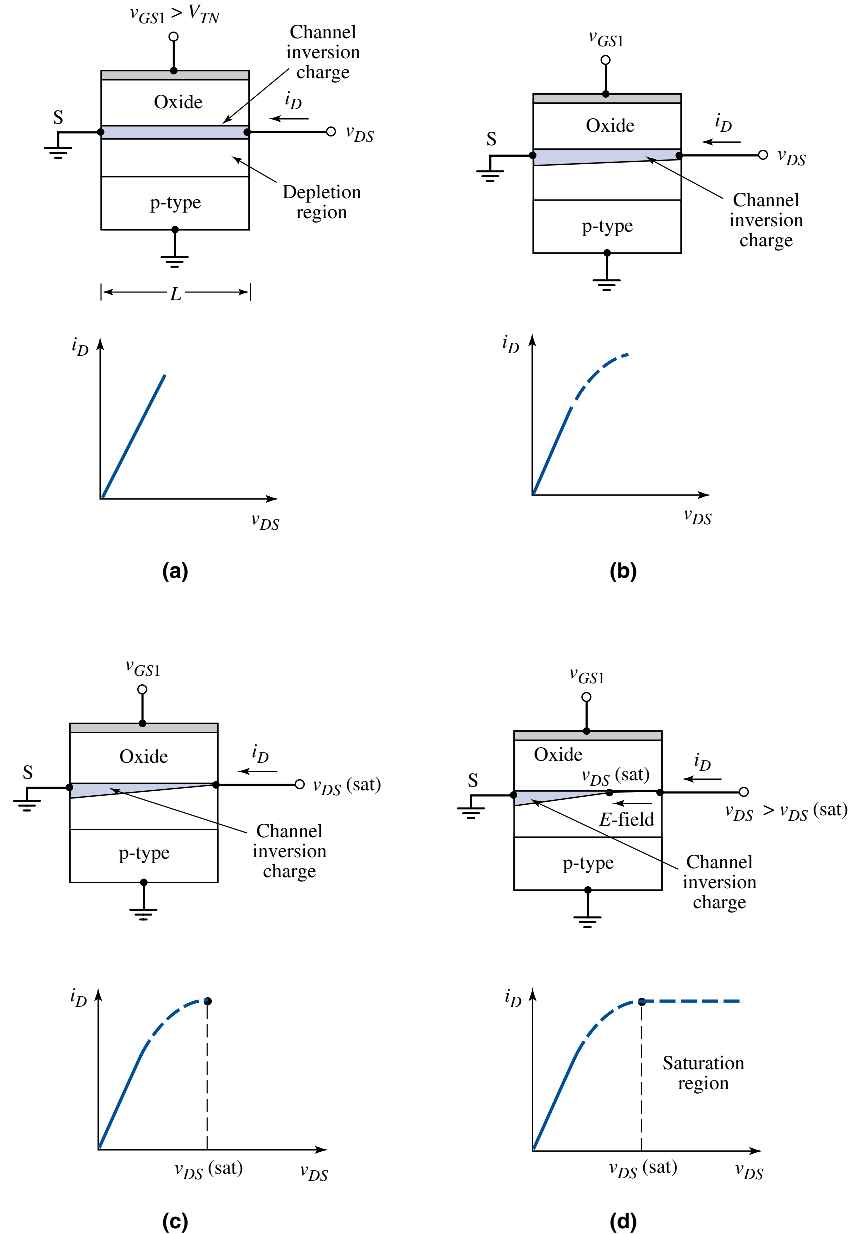


Figure 5.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for: (a) a small v_{DS} value, (b) a larger v_{DS} value, (c) $v_{DS} = v_{DS}(\text{sat})$, and (d) $v_{DS} > v_{DS}(\text{sat})$

As the applied gate-to-source voltage changes, the i_D versus v_{DS} curve changes. In Figure 5.8, we saw that the initial slope of i_D versus v_{DS} increases as v_{GS} increases. Also, Equation (5.1(b)) shows that $v_{DS}(\text{sat})$ is a function of v_{GS}. Therefore, we can generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure 5.10.

Although the derivation of the current–voltage characteristics of the MOSFET is beyond the scope of this text, we can define the relationships.

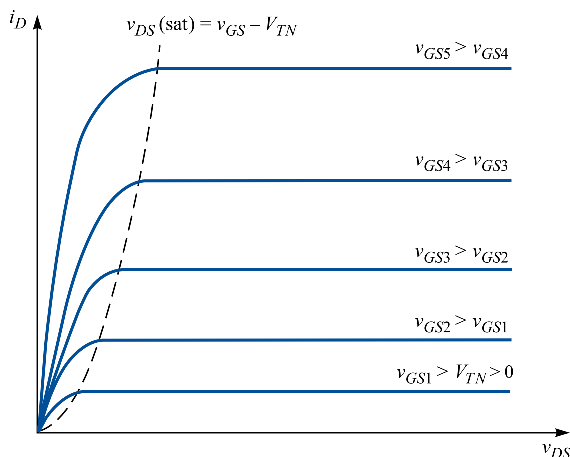


Figure 5.10 Family of i_D versus v_{DS} curves for an n-channel enhancement mode MOSFET

The region for which $v_{DS} < v_{DS}(\text{sat})$ is known as the **nonsaturation** or **triode region**. The ideal current–voltage characteristics in this region are described by the equation

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \quad \textbf{(5.2(a))}$$

In the saturation region, the ideal current–voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation

$$i_D = K_n(v_{GS} - V_{TN})^2 \quad \textbf{(5.2(b))}$$

In the saturation region, since the ideal drain current is independent of the drain-to-source voltage, the incremental or small-signal resistance is infinite. We see that

$$r_o = \Delta v_{DS}/\Delta i_D|_{v_{GS}=\text{const.}} = \infty$$

The parameter K_n is called the **conduction parameter** for the n-channel device and is given by

$$K_n = \frac{W\mu_n C_{ox}}{2L} \quad \textbf{(5.3(a))}$$

where C_{ox} is the oxide capacitance per unit area. The capacitance is given by

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. The parameter μ_n is the mobility of the electrons in the inversion layer. The channel width W and channel length L were shown in Figure 5.5(a).

As Equation (5.3(a)) indicates, the conduction parameter is a function of both electrical and geometric parameters. The oxide capacitance and carrier mobility are essentially constants for a given fabrication technology. However, the geometry, or width-to-length ratio W/L, is a variable in the design of MOSFETs that is used to produce specific current–voltage characteristics in MOSFET circuits.

We can rewrite the conduction parameter in the form

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} \tag{5.3(b)}$$

where $k_n' = \mu_n C_{ox}$. Normally, k_n' is considered to be a constant, so Equation (5.3(b)) emphasizes that the width-to-length ratio W/L is the transistor design variable.

Example 5.1 **Objective:** Calculate the current in an n-channel MOSFET.

Consider an n-channel enhancement mode MOSFET with the following parameters: $V_{TN} = 0.75\,\text{V}$, $W = 40\,\mu\text{m}$, $L = 4\,\mu\text{m}$, $\mu_n = 650\,\text{cm}^2/\text{V–s}$, $t_{ox} = 450\,\text{Å}$, and $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. Determine the current when $V_{GS} = 2V_{TN}$, for the transistor biased in the saturation region.

Solution: The conduction parameter is determined by Equation (5.3(a)). First, consider the units involved in this equation, as follows:

$$K_n = \frac{W(\text{cm}) \cdot \mu_n\left(\dfrac{\text{cm}^2}{\text{V–s}}\right)\epsilon_{ox}\left(\dfrac{\text{F}}{\text{cm}}\right)}{2L(\text{cm}) \cdot t_{ox}(\text{cm})} = \frac{\text{F}}{\text{V–s}} = \frac{(\text{C/V})}{\text{V–s}} = \frac{\text{A}}{\text{V}^2}$$

The value of the conduction parameter is therefore

$$K_n = \frac{W\mu_n\epsilon_{ox}}{2Lt_{ox}} = \frac{(40 \times 10^{-4})(650)(3.9)(8.85 \times 10^{-14})}{2(4 \times 10^{-4})(450 \times 10^{-8})}$$

or

$$K_n = 0.249\,\text{mA/V}^2$$

From Equation (5.2(b)) for $v_{GS} = 2V_{TN}$, we find

$$i_D = K_n(v_{GS} - V_{TN})^2 = (0.249)(1.5 - 0.75)^2 = 0.140\,\text{mA}$$

Comment: The current capability of a transistor can be increased by increasing the conduction parameter. For a given fabrication technology, K_n is adjusted by varying the transistor width W.

Test Your Understanding

5.1 (a) An n-channel enhancement-mode MOSFET has a threshold voltage of $V_{TN} = 1.2\,\text{V}$ and an applied gate-to-source voltage of $v_{GS} = 2\,\text{V}$. Determine the region of operation when: (i) $v_{DS} = 0.4\,\text{V}$; (ii) $v_{DS} = 1\,\text{V}$; and (iii) $v_{DS} = 5\,\text{V}$. (b) Repeat part (a) for an n-channel depletion-mode MOSFET with a threshold voltage of $V_{TN} = -1.2\,\text{V}$. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) (i) nonsaturation, (ii) nonsaturation, (iii) saturation)

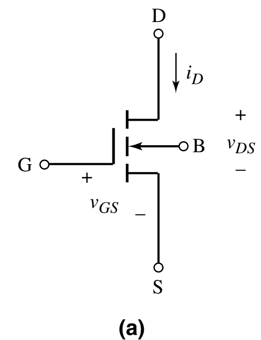
5.2 The NMOS devices described in Exercise 5.1 have parameters $W = 100\,\mu\text{m}$, $L = 7\,\mu\text{m}$, $t_{ox} = 450\,\text{Å}$, $\mu_n = 500\,\text{cm}^2/\text{V–s}$, and $\lambda = 0$. (a) Calculate the conduction parameter K_n for each device. (b) Calculate the drain current for each bias condition. (Ans. (a) $K_n = 0.274\,\text{mA/V}^2$ (b) $i_D = 0.132$, 0.175, and 0.175 mA; $i_D = 0.658$, 1.48, and 2.81 mA)

5.3 An NMOS transistor with $V_{TN} = 1\,\text{V}$ has a drain current $i_D = 0.8\,\text{mA}$ when $v_{GS} = 3\,\text{V}$ and $v_{DS} = 4.5\,\text{V}$. Calculate the drain current when: (a) $v_{GS} = 2\,\text{V}$, $v_{DS} = 4.5\,\text{V}$; and (b) $v_{GS} = 3\,\text{V}$, $v_{DS} = 1\,\text{V}$. (Ans. (a) 0.2 mA (b) 0.6 mA)

5.1.4 Circuit Symbols and Conventions

The conventional circuit symbol for the n-channel enhancement-mode MOSFET is shown in Figure 5.11(a). The vertical solid line denotes the gate electrode, the vertical broken line denotes the channel (the broken line indicates the device is enhancement mode), and the separation between the gate line and channel line denotes the oxide that insulates the gate from the channel. The polarity of the pn junction between the substrate and the channel is indicated by the arrowhead on the body or substrate terminal. The direction of the arrowhead indicates the type of transistor, which in this case is an n-channel device.

In most applications in this text, we will implicitly assume that the source and substrate terminals are connected together. Explicitly drawing the substrate terminal for each transistor in a circuit becomes redundant and makes the circuits appear more complex. Instead, we will use the simplified circuit symbol for the n-channel MOSFET shown in Figure 5.11(b). In this symbol, the arrowhead is on the source terminal and it indicates the direction of current, which for the n-channel device is out of the source. By including the arrowhead in the symbol, we do not need to explicitly indicate the source and drain terminals. We will use the simplified circuit symbol throughout the text except in specific applications.



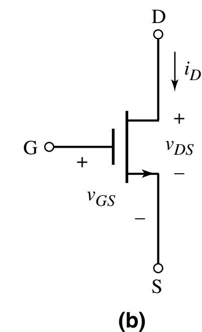


Figure 5.11 The n-channel enhancement-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

5.1.5 Additional MOSFET Structures and Circuit Symbols

Before we start analyzing MOSFET circuits, there are a number of other MOSFET structures in addition to the n-channel enhancement-mode device that need to be considered.

n-Channel Depletion-Mode MOSFET

Figure 5.12(a) shows the cross section of an n-channel **depletion-mode** MOSFET. When zero volts are applied to the gate, an n-channel region or inversion layer exists under the oxide as a result, for example, of impurities introduced during device fabrication. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term **depletion mode** means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

Figure 5.12(b) shows the n-channel depletion mode MOSFET with a negative applied gate-to-source voltage. A negative gate voltage induces a space-charge region under the oxide, thereby reducing the thickness of the n-channel region. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. When the gate voltage is equal to the threshold voltage, which is negative for this device, the induced space-charge region

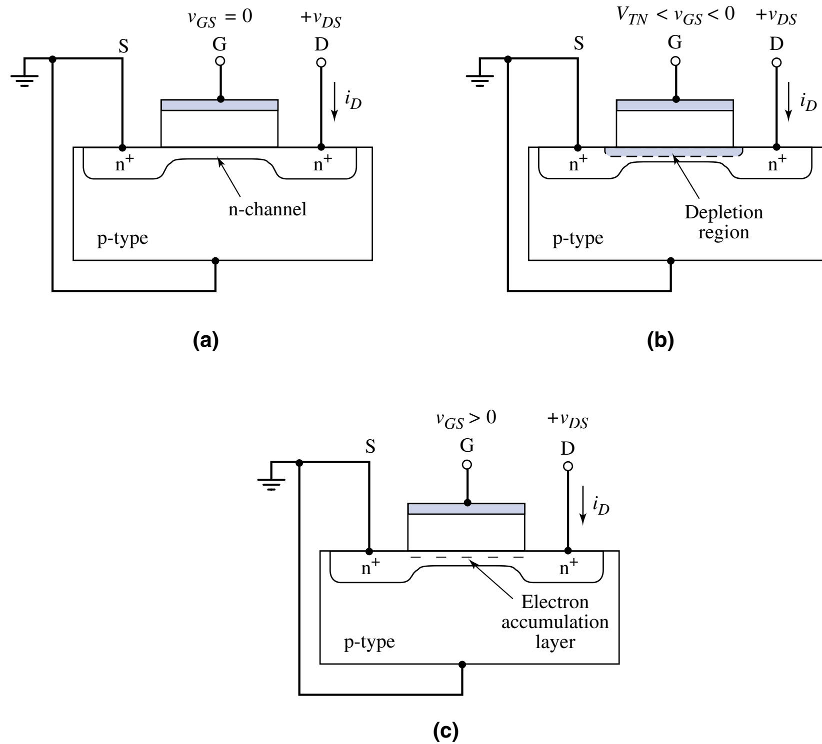


Figure 5.12 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

extends completely through the n-channel region, and the current goes to zero. A positive gate voltage creates an electron accumulation layer, as shown in Figure 5.12(c) which increases the drain current. The general i_D versus v_{DS} family of curves for the n-channel depletion-mode MOSFET is shown in Figure 5.13.

The current–voltage characteristics defined by Equations (5.2(a)) and (5.2(b)) apply to both enhancement- and depletion-mode n-channel devices. The only difference is that the threshold voltage V_{TN} is positive for the enhancement-mode MOSFET and negative for the depletion-mode MOSFET. Even though the current–voltage characteristics of enhancement- and depletion-mode devices are described by the same equations, different circuit symbols are used, simply for purposes of clarity.

The conventional circuit symbol for the n-channel depletion-mode MOSFET is shown in Figure 5.14(a). The vertical solid line denoting the channel indicates the device is depletion mode. A comparison of Figures 5.11(a) and 5.14(a) shows that the only difference between the enhancement- and depletion-mode symbols is the broken versus the solid line representing the channel.

A simplified symbol for the n-channel depletion-mode MOSFET is shown in Figure 5.14(b). The arrowhead is again on the source terminal and indicates the direction of current, which for the n-channel device is out of the source. The heavy solid line represents the depletion-mode channel region. Again,

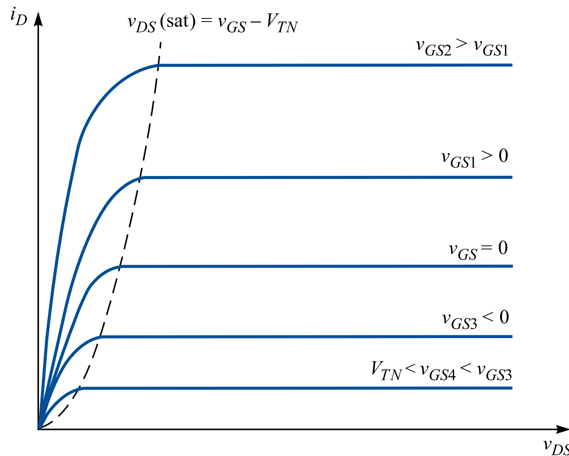


Figure 5.13 Family of i_D vesus v_{DS} curves for an n-channel depletion mode MOSFET

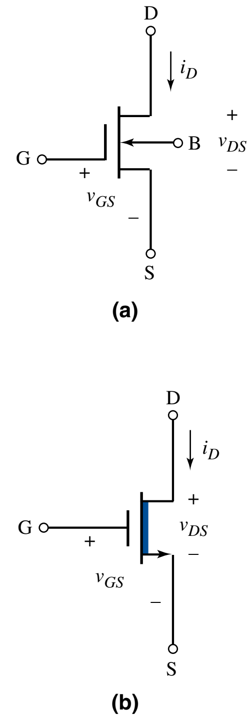


Figure 5.14 The n-channel depletion-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

using a different circuit symbol for the depletion-mode device compared to the enhancement-mode device is simply for clarity in a circuit diagram.

p-Channel MOSFETs

Figures 5.15(a) and 5.15(b) show cross sections of a p-channel enhancement-mode and a p-channel depletion-mode MOSFET, as well as the biasing configurations and currrent directions. The types of impurity doping in the source, drain, and substrate regions of the **p-channel MOSFET**, or **PMOS transistor**, are reversed compared to the n-channel device. In the p-channel enhancement-mode device, a negative gate-to-source voltage must be applied to create the inversion layer, or channel region, of holes that "connects" the source and drain regions. The threshold voltage, denoted as V_{TP} for the p-channel device,[4] is negative for an enhancement-mode device. The threshold voltage V_{TP} is positive for a p-channel depletion-mode device. Because holes flow from the source to the drain, the conventional current enters the source and leaves the drain. A p-channel region exists in the depletion-mode device with zero gate voltage.

The operation of the p-channel device is the same as that of the n-channel device, except that the hole is the charge carrier, rather than the electron, and the conventional current direction and voltage polarities are reversed. For the p-channel device biased in the nonsaturation region, the current is given by

$$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2] \tag{5.4(a)}$$

In the saturation region, the current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2 \tag{5.4(b)}$$

[4]Using a different threshold voltage parameter for a PMOS device compared to that for the NMOS device is simply for clarity in particular applications.

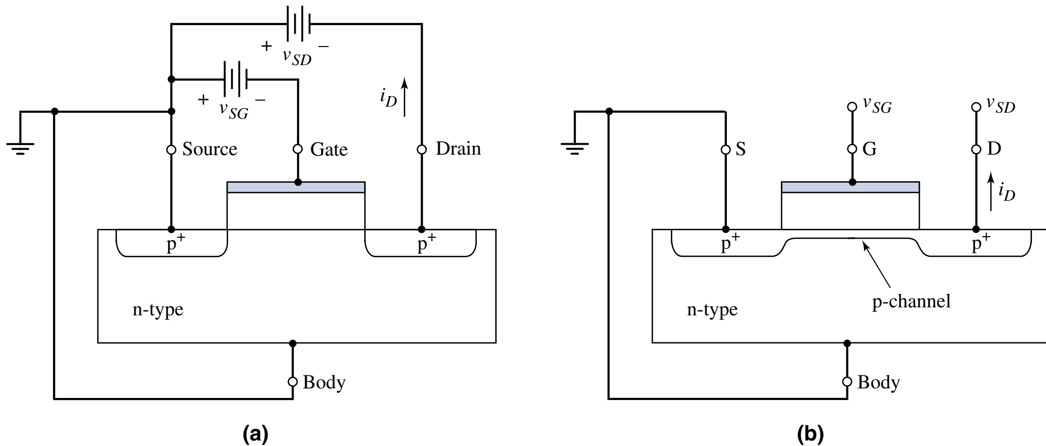


Figure 5.15 Cross section of p-channel MOSFETs: (a) enhancement-mode and (b) depletion-mode

and the drain current exits the drain terminal. The parameter K_p is the conduction parameter for the p-channel device and is given by

$$K_p = \frac{W\mu_p C_{ox}}{2L} \tag{5.5(a)}$$

where W, L, and C_{ox} are the channel width, length, and oxide capacitance per unit area, as previously defined. The parameter μ_p is the mobility of holes in the hole inversion layer. In general, the hole inversion layer mobility is less than the electron inversion layer mobility.

We can also rewrite Equation (5.5(a)) in the form

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L} \tag{5.5(b)}$$

where $k_p' = \mu_p C_{ox}$.

For a p-channel MOSFET biased in the saturation region, we have

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} \tag{5.6}$$

Example 5.2 **Objective:** Determine the source-to-drain voltage required to bias a p-channel depletion-mode MOSFET in the saturation region.

Consider a depletion-mode p-channel MOSFET for which $K_p = 0.2\,\text{mA/V}^2$, $V_{TP} = +0.50\,\text{V}$, and $i_D = 0.50\,\text{mA}$.

Solution: In the saturation region, the drain current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$

or

$$0.50 = 0.2(v_{SG} + 0.50)^2$$

which yields

$$v_{SG} = 1.08\,\text{V}$$

To bias this p-channel MOSFET in the saturation region, the following must apply:

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} = 1.08 + 0.5 = 1.58\text{ V}$$

Comment: Biasing a transistor in either the saturation or the nonsaturation region depends on both the gate-to-source voltage and the drain-to-source voltage.

Test Your Understanding

5.4 (a) For a PMOS device, the threshold voltage is $V_{TP} = -2$ V and the applied source-to-gate voltage is $v_{SG} = 3$ V. Determine the region of operation when: (i) $v_{SD} = 0.5$ V; (ii) $v_{SD} = 2$ V; and (iii) $v_{SD} = 5$ V. (b) Repeat part (a) for a depletion-mode PMOS device with $V_{TP} = +0.5$ V. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) nonsaturation, (ii) nonsaturation, (iii) saturation)

The conventional circuit symbol for the p-channel enhancement-mode MOSFET appears in Figure 5.16(a). Note that the arrowhead direction on the substrate terminal is reversed from that in the n-channel enhancement-mode device. The simplified circuit symbol we will use is shown in Figure 5.16(b). The arrowhead is on the source terminal, indicating the direction of current, which for the p-channel device is into the source.

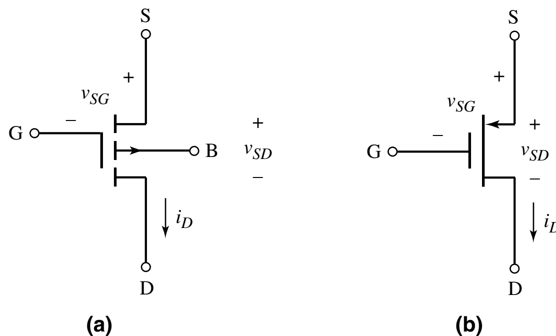


Figure 5.16 The p-channel enhancement-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

The conventional and simplified circuit symbols for the p-channel depletion-mode device are shown in Figure 5.17. The heavy solid line in the simplified symbol represents the channel region and denotes the depletion-mode device. The arrowhead is again on the source terminal and it indicates the current direction.

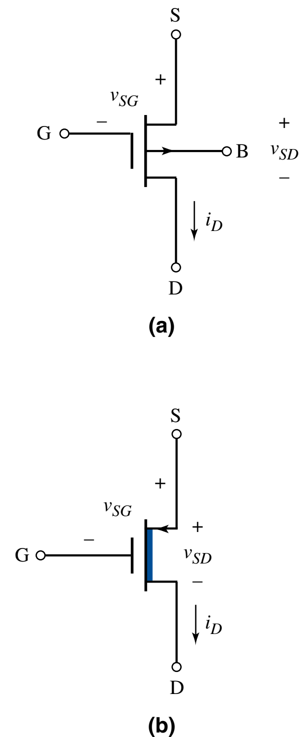


Figure 5.17 The p-channel depletion mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

Complementary MOSFETs

Complementary MOS (CMOS) technology uses both n-channel and p-channel devices in the same circuit. Figure 5.18 shows the cross section of n-channel and p-channel devices fabricated on the same chip. CMOS circuits, in general,

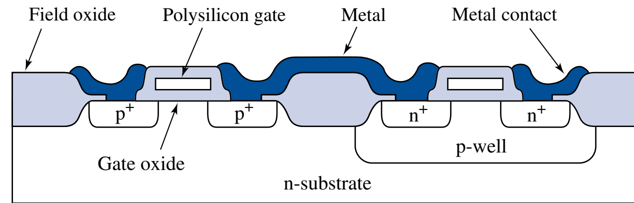


Figure 5.18 Cross sections of n-channel and p-channel transistors fabricated with a p-well CMOS technology

are more complicated to fabricate than circuits using entirely NMOS or PMOS devices. Yet, as we will see in later chapters, CMOS circuits have great advantages over just NMOS or PMOS circuits.

In order to fabricate n-channel and p-channel devices that are electrically equivalent, the magnitude of the threshold voltages must be equal, and the n-channel and p-channel conduction parameters must be equal. Since, in general, μ_n and μ_p are not equal, the design of equivalent transistors involves adjusting the width-to-length ratios of the transistors.

5.1.6 Summary of Transistor Operation

We have presented a first-order model of the operation of the MOS transistor. For an n-channel enhancement-mode MOSFET, a positive gate-to-source voltage, greater than the threshold voltage V_{TN}, must be applied to induce an electron inversion layer. For $v_{GS} > V_{TN}$, the device is turned on. For an n-channel depletion-mode device, a channel between the source and drain exists even for $v_{GS} = 0$. The threshold voltage is negative, so that a negative value of v_{GS} is required to turn the device off.

For a p-channel device, all voltage polarities and current directions are reversed compared to the NMOS device. For the p-channel enhancement-mode transistor, $V_{TP} < 0$ and for the depletion-mode PMOS transistor, $V_{TP} > 0$.

Table 5.1 lists the first-order equations that describe the *i*–*v* relationships in MOS devices. We note that K_n and K_p are positive values and that the drain current i_D is positive into the drain for the NMOS device and positive out of the drain for the PMOS device.

Table 5.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

5.1.7 Nonideal Current–Voltage Characteristics

The five nonideal effects in the current–voltage characteristics of MOS transistors are: the finite output resistance in the saturation region, the body effect, subthreshold conduction, breakdown effects, and temperature effects. This section will examine each of these effects.

Finite Output Resistance

In the ideal case, when a MOSFET is biased in the saturation region, the drain current i_D is independent of drain-to-source voltage v_{DS}. However, in actual MOSFET i_D versus v_{DS} characteristics, a nonzero slope does exist beyond the saturation point. For $v_{DS} > v_{DS}(\text{sat})$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal (see Figure 5.9(d)). The effective channel length decreases, producing the phenomenon called **channel length modulation**.

An exaggerated view of the current–voltage characteristics is shown in Figure 5.19. The curves can be extrapolated so that they intercept the voltage axis at a point $v_{DS} = -V_A$. The voltage V_A is usually defined as a positive quantity and is similar to the Early voltage of a bipolar transistor (see Chapter 3). The slope of the curve in the saturation region can be described by expressing the i_D versus v_{DS} characteristic in the form, for an n-channel device,

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \quad \textbf{(5.7)}$$

where λ is a positive quantity called the channel-length modulation parameter.

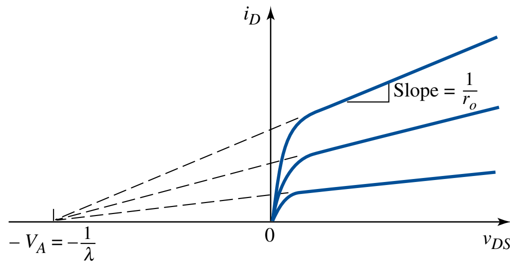


Figure 5.19 Effect of channel length modulation, resulting in a finite output resistance

The parameters λ and V_A are related. From Equation (5.7), we have $(1 + \lambda v_{DS}) = 0$ at the extrapolated point where $i_D = 0$. At this point, $v_{DS} = -V_A$, which means that $V_A = 1/\lambda$.

The output resistance due to the channel length modulation is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \quad \textbf{(5.8)}$$

From Equation (5.7), the output resistance, evaluated at the Q-point, is

$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1} \quad \textbf{(5.9(a))}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}} \tag{5.9(b)}$$

The output resistance r_o is also a factor in the small-signal equivalent circuit of the MOSFET, which is discussed in the next chapter.

Test Your Understanding

5.5 For an NMOS enhancement-mode device, the parameters are: $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$. The device is biased at $v_{GS} = 2.5\,\text{V}$. Calculate the drain current when $v_{DS} = 2\,\text{V}$ and $v_{DS} = 10\,\text{V}$ for: (a) $\lambda = 0$ and (b) $\lambda = 0.02\,\text{V}^{-1}$. (c) Calculate the output resistance r_o for parts (a) and (b). (Ans. (a) $i_D = 0.289\,\text{mA}$ for both 2 and 10 V; (b) $i_D = 0.30\,\text{mA}$ (2 V), $i_D = 0.347\,\text{mA}$ (10 V); (c) $r_o = \infty$ (a), $r_o = 173\,\text{k}\Omega$ (b))

Body Effect

Up to this point, we have assumed that the substrate, or body, is connected to the source. For this bias condition, the threshold voltage is a constant.

In integrated circuits, however, the substrates of all n-channel MOSFETs are usually common and are tied to the most negative potential in the circuit. An example of two n-channel MOSFETs in series is shown in Figure 5.20. The p-type substrate is common to the two transistors, and the drain of M_1 is common to the source of M_2. When the two transistors are conducting, there is a nonzero drain-to-source voltage on M_1, which means that the source of M_2 is not at the same potential as the substrate. These bias conditions mean that a zero or reverse-bias voltage exists across the source–substrate pn junction, and a change in the source–substrate junction voltage changes the threshold voltage. This is called the **body effect**. The same situation exists in p-channel devices.

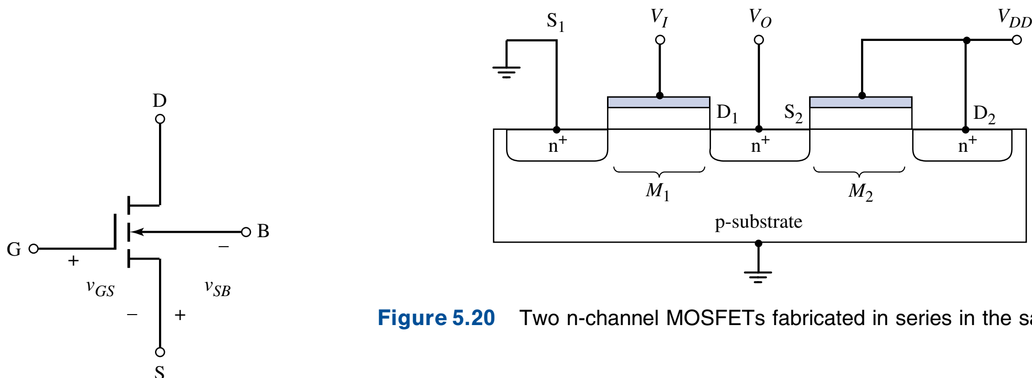


Figure 5.20 Two n-channel MOSFETs fabricated in series in the same substrate

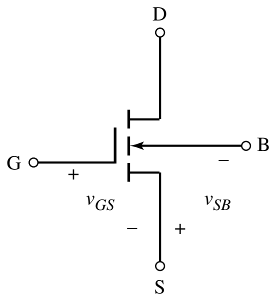


Figure 5.21 An n-channel enhancement-mode MOSFET with a substrate voltage

For example, consider the n-channel device shown in Figure 5.21. To maintain a zero- or reverse-biased source–substrate pn junction, we must have $v_{SB} \geq 0$. The threshold voltage for this condition is given by

$$V_{TN} = V_{TNO} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right] \quad \textbf{(5.10)}$$

where V_{TNO} is the threshold voltage for $v_{SB} = 0$; γ, called the bulk threshold or **body-effect parameter**, is related to device properties, and is typically on the order of $0.5\ \text{V}^{1/2}$; and ϕ_f is a semiconductor parameter, typically on the order of 0.35 V, and is a function of the semiconductor doping. We see from Equation (5.10) that the threshold voltage in n-channel devices increases due to this body effect.

The body effect can cause a degradation in circuit performance because of the changing threshold voltage. However, we will generally neglect the body effect in our circuit analyses, for simplicity.

Test Your Understanding

5.6 An NMOS transistor has parameters $V_{TNO} = 1$ V, $\gamma = 0.35\ \text{V}^{1/2}$, and $\phi_f = 0.35$ V. Calculate the threshold voltage when: (a) $v_{SB} = 0$, (b) $v_{SB} = 1$ V, and (c) $v_{SB} = 4$ V. (Ans. (a) 1 V, (b) 1.16 V, (c) 1.47 V)

Subthreshold Conduction

If we consider the ideal current-voltage relationship for the n-channel MOSFET biased in the saturation region, we have, from Equation (5.2(b)),

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Taking the square root of both sides of the equation, we obtain

$$\sqrt{i_D} = \sqrt{K_n}(v_{GS} - V_{TN}) \quad \textbf{(5.11)}$$

From Equation (5.11), we see that $\sqrt{i_d}$ is a linear function of v_{GS}. Figure 5.22 shows a plot of this ideal relationship.

Also plotted in Figure 5.22 are experimental results, which show that when v_{GS} is slightly less than V_{TN}, the drain current is not zero, as previously assumed. This current is called the **subthreshold current**. The effect may not be significant for a single device, but if hundreds or thousands of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit. One example of this is a dynamic random access memory (DRAM), as we will see in Chapter 16.

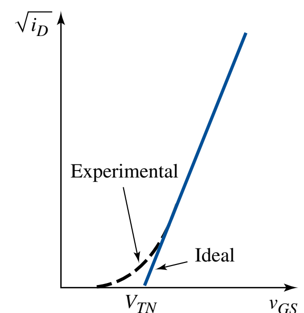


Figure 5.22 Plot of $\sqrt{i_D}$ versus v_{GS} characteristic showing subthreshold conduction

In this text, for simplicity we will not specifically consider the subthreshold current. However, when a MOSFET in a circuit is to be turned off, the "proper" design of the circuit must involve biasing the device at least a few tenths of a volt below the threshold voltage to achieve "true" cutoff.

Breakdown Effects

Several possible breakdown effects may occur in a MOSFET. The drain-to-substrate pn junction may break down if the applied drain voltage is too high

and avalanche multiplication occurs. This breakdown is the same reverse-biased pn junction breakdown discussed in Chapter 1 in Section 1.2.5.

As the size of the device becomes smaller, another breakdown mechanism, called *punch-through*, may become significant. **Punch-through** occurs when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. This effect also causes the drain current to increase rapidly with only a small increase in drain voltage.

A third breakdown mechanism is called **near-avalanche** or **snapback breakdown**. This breakdown process is due to second-order effects within the MOSFET. The source-substrate-drain structure is equivalent to that of a bipolar transistor. As the device size shrinks, we may begin to see a parasitic bipolar transistor action with increases in the drain voltage. This parasitic action enhances the breakdown effect.

If the electric field in the oxide becomes large enough, breakdown can also occur in the oxide, which can lead to catastrophic failure. In silicon dioxide, the electric field at breakdown is on the order of 6×10^6 V/cm, which, to a first approximation, is given by $E_{ox} = V_G/t_{ox}$. A gate voltage of approximately 30 V would produce breakdown in an oxide with a thickness of $t_{ox} = 500$ Å. However, a safety margin of a factor of 3 is common, which means that the maximum safe gate voltage for $t_{ox} = 500$ Å would be 10 V. A safety margin is necessary since there may be defects in the oxide that lower the breakdown field. We must also keep in mind that the input impedance at the gate is very high, and a small amount of static charge accumulating on the gate can cause the breakdown voltage to be exceeded. To prevent the accumulation of static charge on the gate capacitance of a MOSFET, a gate protection device, such as a reverse-biased diode, is usually included at the input of a MOS integrated circuit.

Temperature Effects

Both the threshold voltage V_{TN} and conduction parameter K_n are functions of temperature. The magnitude of the threshold voltage decreases with temperature, which means that the drain current increases with temperature at a given V_{GS}. However, the conduction parameter is a direct function of the inversion carrier mobility, which decreases as the temperature increases. Since the temperature dependence of mobility is larger than that of the threshold voltage, the net effect of increasing temperature is a decrease in drain current at a given V_{GS}. This particular result provides a negative feedback condition in power MOSFETs. A decreasing value of K_n inherently limits the channel current and provides stability for a power MOSFET.

5.2 MOSFET DC CIRCUIT ANALYSIS

In the last section, we considered the basic MOSFET characteristics and properties. We now start analyzing and designing the dc biasing of MOS transistor circuits. A primary purpose of the rest of the chapter is to continue to become familiar and comfortable with the MOS transistor and MOSFET circuits. As with bipolars, the dc biasing of MOSFETs, the focus of this chapter, is an

important part of the design of amplifiers. MOSFET amplifier design is the focus of the next chapter.

In most of the circuits presented in this chapter, resistors are used in conjunction with the MOS transistors. In a real MOSFET integrated circuit, however, the resistors are generally replaced by other MOSFETs, so the circuit is composed entirely of MOS devices. As we go through the chapter, we will begin to see how this is accomplished and as we finish the text, we will indeed analyze and design circuits containing only MOSFETs.

In the dc analysis of MOSFET circuits, we can use the ideal current–voltage equations listed in Table 5.1 in Section 5.1.

5.2.1 Common-Source Circuit

One of the basic MOSFET circuit configurations is called the **common-source circuit**. Figure 5.23 shows one example of this type of circuit using an n-channel enhancement-mode MOSFET. The source terminal is at ground potential and is common to both the input and output portions of the circuit. The coupling capacitor C_C acts as an open circuit to dc but it allows the signal voltage to be coupled to the gate of the MOSFET.

The dc equivalent circuit is shown in Figure 5.24(a). In the following dc analyses, we again use the notation for dc currents and voltages. Since the gate current into the transistor is zero, the voltage at the gate is given by a voltage divider, which can be written as

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \tag{5.12}$$

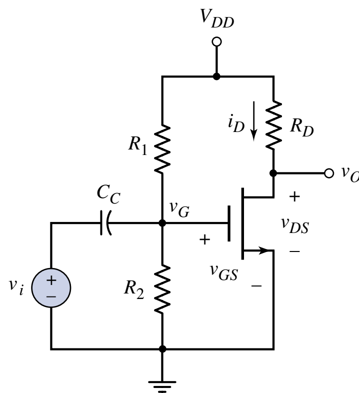
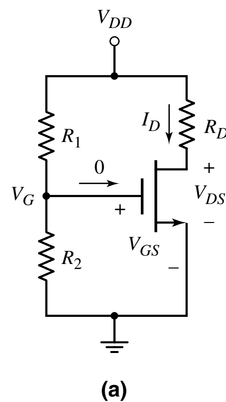


Figure 5.23 An NMOS common-source circuit



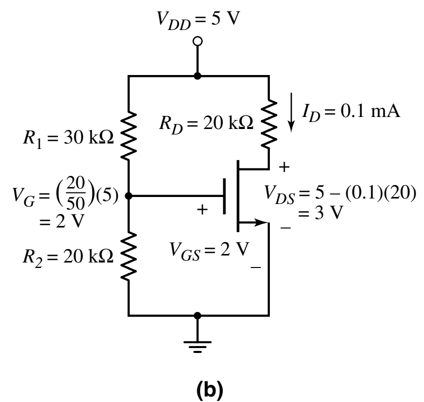


Figure 5.24 (a) An NMOS common-source circuit and (b) the NMOS circuit for Example 5.3

Assuming that the gate-to-source voltage given by Equation (5.12) is greater than V_{TN}, and that the transistor is biased in the saturation region, the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 \tag{5.13}$$

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D \quad \textbf{(5.14)}$$

If $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$, then the transistor is biased in the saturation region, as we initially assumed, and our analysis is correct. If $V_{DS} < V_{DS}(\text{sat})$, then the transistor is biased in the nonsaturation region, and the drain current is given by Equation (5.2(a)).

Example 5.3 **Objective:** Calculate the drain current and drain-to-source voltage of a common-source circuit with an n-channel enhancement-mode MOSFET.

For the circuit shown in Figure 5.24(a), assume that $R_1 = 30\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_D = 20\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $V_{TN} = 1\,\text{V}$, and $K_n = 0.1\,\text{mA/V}^2$.

Solution: From the circuit shown in Figure 5.24(b) and Equation (5.12), we have

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{20}{20 + 30}\right)(5) = 2\,\text{V}$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (0.1)(2 - 1)^2 = 0.1\,\text{mA}$$

and the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3\,\text{V}$$

Comment: Because $V_{DS} = 3\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2 - 1 = 1\,\text{V}$, the transistor is indeed biased in the saturation region and our analysis is valid.

Figure 5.25(a) shows a common-source circuit with a p-channel enhancement-mode MOSFET. The source terminal is tied to $+V_{DD}$, which becomes signal ground in the ac equivalent circuit. Thus the terminology common-source applies to this circuit.

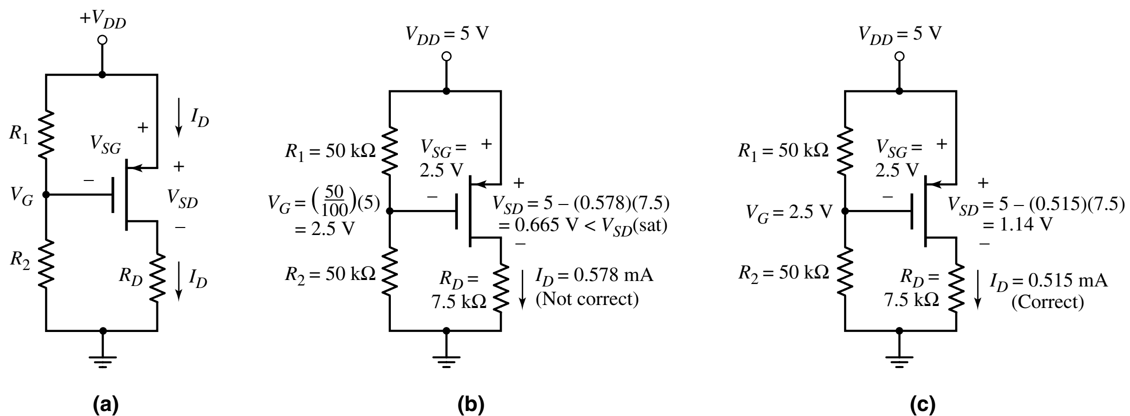


Figure 5.25 (a) A PMOS common-source circuit, (b) results when saturation-region bias assumption is incorrect, and (c) results when nonsaturation-region bias assumption is correct

The dc analysis is essentially the same as for the n-channel MOSFET circuit. The gate voltage is

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) \tag{5.15(a)}$$

and the source-to-gate voltage is

$$V_{SG} = V_{DD} - V_G \tag{5.15(b)}$$

Assuming that $V_{GS} < V_{TP}$, or $V_{SG} > |V_{TP}|$, and that the device is biased in the saturation region, the drain current is given by

$$I_D = K_p(V_{SG} + V_{TP})^2 \tag{5.16}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D \tag{5.17}$$

If $V_{SD} > V_{SD}(\text{sat}) = V_{SG} + V_{TP}$, then the transistor is indeed biased in the saturation region, as we have assumed. However, if $V_{SD} < V_{SD}(\text{sat})$, the transistor is biased in the nonsaturation region.

Example 5.4 **Objective:** Calculate the drain current and source-to-drain voltage of a common-source circuit with a p-channel enhancement-mode MOSFET.

Consider the circuit shown in Figure 5.25(a). Assume that $R_1 = R_2 = 50\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $R_D = 7.5\,\text{k}\Omega$, $V_{TP} = -0.8\,\text{V}$, and $K_p = 0.2\,\text{mA/V}^2$.

Solution: From the circuit shown in Figure 5.25(b) and Equation (5.15(a)), we have

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{50}{50 + 50}\right)(5) = 2.5\,\text{V}$$

The source-to-gate voltage is therefore

$$V_{SG} = V_{DD} - V_G = 5 - 2.5 = 2.5\,\text{V}$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_p(V_{SG} + V_{TP})^2 = (0.2)(2.5 - 0.8)^2 = 0.578\,\text{mA}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D = 5 - (0.578)(7.5) = 0.665\,\text{V}$$

Since $V_{SD} = 0.665\,\text{V}$ is not greater than $V_{SD}(\text{sat}) = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7\,\text{V}$, the p-channel MOSFET is not biased in the saturation region, as we initially assumed.

In the nonsaturation region, the drain current is given by

$$I_D = K_p[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D$$

Combining these two equations, we obtain

$$I_D = K_p[2(V_{SG} + V_{TP})(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2]$$

or

$$I_D = (0.2)[2(2.5 - 0.8)(5 - I_D(7.5)) - (5 - I_D(7.5))^2]$$

Solving this quadratic equation for I_D, we find

$$I_D = 0.515\,\text{mA}$$

We also find that

$$V_{SD} = 1.14\,\text{V}$$

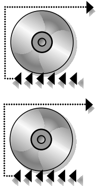
Therefore, $V_{SD} < V_{SD}(\text{sat})$, which verifies that the transistor is biased in the nonsaturation region.

Comment: In solving the quadratic equation for I_D, we find a second solution that yields $V_{SD} = 2.93\,\text{V}$. However, this value of V_{SD} is greater than $V_{SD}(\text{sat})$, so it is not a valid solution since we assumed the transistor to be biased in the nonsaturation region.

As Example 5.4 illustrated, we may not know initially whether a transistor is biased in the saturation or nonsaturation region. The approach involves making an educated guess and then verifying that assumption. If the assumption proves incorrect, we must then change it and reanalyze the circuit.

In linear amplifiers containing MOSFETs, the transistors are biased in the saturation region.

Test Your Understanding



***5.7** For the transistor in the circuit in Figure 5.26, the parameters are $V_{TN} = 1\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$. Determine V_{GS}, I_D, and V_{DS}. (Ans. $V_{GS} = 2.65\,\text{V}$, $I_D = 1.36\,\text{mA}$, $V_{DS} = 5.92\,\text{V}$)

***5.8** Consider the circuit shown in Figure 5.27. The transistor parameters are $V_{TP} = -1\,\text{V}$ and $K_p = 0.25\,\text{mA/V}^2$. Calculate V_{SG}, I_D, and V_{SD}. (Ans. $V_{SG} = 3.04\,\text{V}$, $I_D = 1.04\,\text{mA}$, $V_{SD} = 4.59\,\text{V}$)

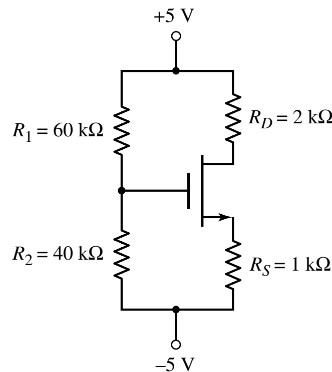


Figure 5.26 Circuit for Exercise 5.7

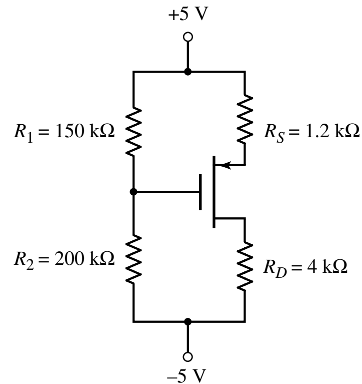


Figure 5.27 Circuit for Exercise 5.8

RD5.9 The transistor in the circuit shown in Figure 5.24(a) has parameters $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.25\,\text{mA/V}^2$. The circuit is biased with $V_{DD} = 7.5\,\text{V}$. Let $R_1 + R_2 = 250\,\text{k}\Omega$. Redesign the circuit such that $I_D = 0.40\,\text{mA}$ and $V_{DS} = 4\,\text{V}$ (Ans. $R_2 = 68.7\,\text{k}\Omega$, $R_1 = 181.3\,\text{k}\Omega$, $R_D = 8.75\,\text{k}\Omega$)

5.2.2 Load Line and Modes of Operation

The load line is helpful in visualizing the region in which the MOSFET is biased. Consider again the common-source circuit shown in Figure 5.24(b). Writing a Kirchhoff's voltage law equation around the drain–source loop results in Equation (5.14), which is the load line equation, showing a linear relationship between the drain current and drain-to-source voltage.

Figure 5.28 shows the v_{DS}(sat) characteristic for the transistor described in Example 5.3. The load line is given by

$$V_{DS} = V_{DD} - I_D R_D = 5 - I_D(20) \tag{5.18(a)}$$

or

$$I_D = \frac{5}{20} - \frac{V_{DS}}{20} \text{ (mA)} \tag{5.18(b)}$$

and is also plotted in the figure. The two end points of the load line are determined in the usual manner. If $I_D = 0$, then $V_{DS} = 5\,\text{V}$; if $V_{DS} = 0$, then $I_D = 5/20 = 0.25\,\text{mA}$. The Q-point of the transistor is given by the dc drain current and drain-to-source voltage, and it is always on the load line, as shown in the figure. A few transistor characteristics are also shown on the figure.

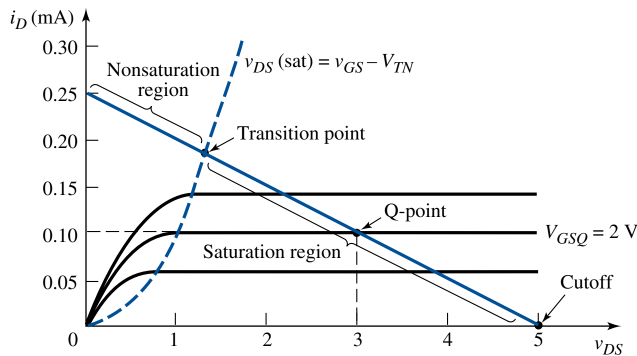


Figure 5.28 Transistor characteristics, v_{DS}(sat) curve, load line, and Q-point for the NMOS common-source circuit in Figure 5.24(b)

If the gate-to-source voltage is less than V_{TN}, the drain current is zero and the transistor is in cutoff. As the gate-to-source voltage becomes just greater than V_{TN}, the transistor turns on and is biased in the saturation region. As V_{GS} increases, the Q-point moves up the load line. The **transition point** is the boundary between the saturation and nonsaturation regions and is defined as the point where $V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_{TN}$. As V_{GS} increase above the transition point value, the transistor becomes biased in the nonsaturation region.

Example 5.5 **Objective:** Determine the transition point parameters for a common-source circuit.

Consider the circuit shown in Figure 5.24(b). Assume transistor parameters of $V_{TN} = 1\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$.

Solution: At the transition point,

$$V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_{TN} = V_{DD} - I_D R_D$$

The drain current is still

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining the last two equations, we obtain

$$V_{GS} - V_{TN} = V_{DD} - K_n R_D (V_{GS} - V_{TN})^2$$

Rearranging this equation produces

$$K_n R_D (V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - V_{DD} = 0$$

or

$$(0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$$

Solving the quadratic equation, we find that

$$V_{GS} - V_{TN} = 1.35\,\text{V} = V_{DS}$$

Therefore,

$$V_{GS} = 2.35\,\text{V}$$

and

$$I_D = (0.1)(2.35 - 1)^2 = 0.182\,\text{mA}$$

Comment: For $V_{GS} < 2.35\,\text{V}$, the transistor is biased in the saturation region; for $V_{GS} > 2.35\,\text{V}$, the transistor is biased in the nonsaturation region.

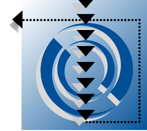
Problem-Solving Technique: MOSFET DC Analysis

Analyzing the dc response of a MOSFET circuit requires knowing the bias condition (saturation or nonsaturation) of the transistor. In some cases, the bias condition may not be obvious, which means that we have to guess the bias condition, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the saturation region, in which case $V_{GS} > V_{TN}$, $I_D > 0$, and $V_{DS} \geq V_{DS}(\text{sat})$.
2. Analyze the circuit using the saturation current-voltage relations.
3. Evaluate the resulting bias condition of the transistor. If the assumed parameter values in step 1 are valid, then the initial assumption is correct. If $V_{GS} < V_{TN}$, then the transistor is probably cutoff, and if $V_{DS} < V_{DS}(\text{sat})$, the transistor is likely biased in the nonsaturation region.
4. If the initial assumption is proved incorrect, then a new assumption must be made and the circuit reanalyzed. Step 3 must then be repeated.

5.2.3 Common MOSFET Configurations: DC Analysis

There are various other MOSFET circuit configurations, in addition to the basic common-source circuit. Several examples are discussed in this section. We continue the dc analysis and design of MOSFET circuits to increase our proficiency and to become more adept in the analysis of these types of circuits.



Design Example 5.6 **Objective:** Design the dc bias of a MOSFET circuit to produce a specified drain current.

For the dc circuit in Figure 5.29, assume the MOSFET parameters are $V_{TN} = 2\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $W/L = 4$. Choose R_1 and R_2 such that the current in the bias resistors is approximately one-tenth of I_D. Design the circuit such that $I_D = 0.5\,\text{mA}$. In the final design, standard resistor values are to be used.

Solution: Assuming the transistor is biased in the saturation region, we have

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$0.5 = \left(\frac{0.080}{2}\right) \cdot (4) \cdot (V_{GS} - 2)^2$$

which yields

$$V_{GS} = 3.77\,\text{V}$$

The current through the bias resistors should be approximately 0.05 mA so that

$$R_1 + R_2 = \frac{10}{0.05} = 200\,\text{k}\Omega$$

We can write

$$V_{GS} = V_G - V_S = \left[\left(\frac{R_2}{R_1 + R_2}\right)(10) - 5\right] - [I_D R_S - 5]$$

so that

$$3.77 = \left(\frac{R_2}{200}\right)(10) - (0.5)(2)$$

We find that

$$R_2 = 95.4\,\text{k}\Omega \quad \text{and} \quad R_1 = 104.6\,\text{k}\Omega$$

The closest standard resistor values are $R_2 = 100\,\text{k}\Omega$ and $R_1 = 110\,\text{k}\Omega$.

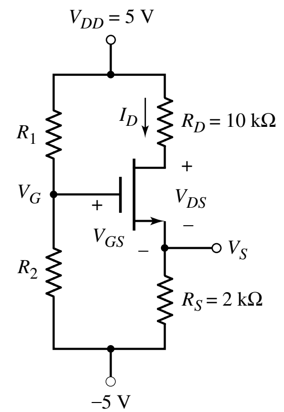
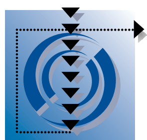


Figure 5.29 NMOS common-source circuit with source resistor

Comment: Since $V_{DS} = 4\,\text{V}$, then $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 3.77 - 2 = 1.77\,\text{V}$. Therefore, the transistor is biased in the saturation region, as initially assumed.

Design Pointer: We must keep in mind that there are certain tolerances in resistor values as well as tolerances in transistor conduction parameter and threshold voltage values. These tolerances lead to variations in the Q-point values. One implication of this variation is that we should not design the Q-point too close to the transition point, or the parameter variations may push the Q-point into the nonsaturation region. This is one situation in which a computer simulation may cut down the number of tedious calculations.

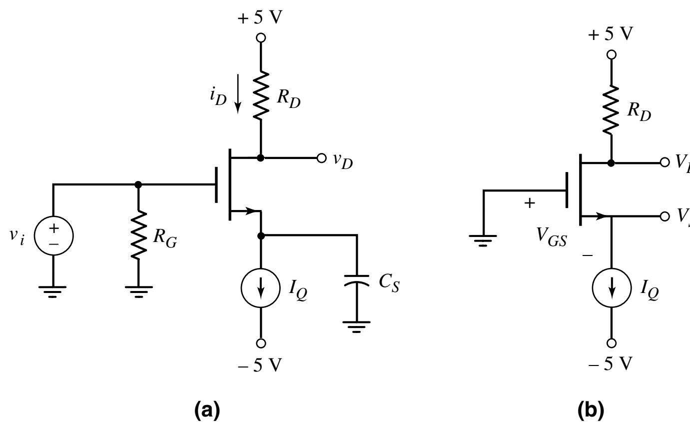
In bipolar circuits, we observed that the Q-point tended to be stabilized when an emitter resistor was included in the circuit. In a similar way, the Q-point of MOSFET circuits will tend to be stabilized against variations in transistor parameters by including a source resistor. The transistor conduction parameter may vary from one device to another because of fabrication tolerances in channel length, channel width, oxide thickness, or carrier mobility. The threshold voltage may also vary from one device to another. Variations in these device parameters will change the Q-point in a given circuit, but the change can be lessened by including a source resistor. Further, in many MOSFET circuits today, the source resistor is replaced by a constant-current source, which biases the transistor with a constant current that is independent of the transistor parameters, thereby stabilizing the Q-point.



Objective: Design a MOSFET circuit biased with a constant-current source.

The parameters of the transistor in the circuit shown in Figure 5.30(a) are $V_{TN} = 0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $W/L = 3$. Design the circuit such that the quiescent values are $I_D = 250\,\mu\text{A}$ and $V_D = 2.5\,\text{V}$.

Solution: The dc equivalent circuit is shown in Figure 5.30(b). Since $v_i = 0$, the gate is at ground potential and there is no gate current through R_G.



(a) NMOS common-source circuit biased with a constant-current source and (b) equivalent dc circuit

Assuming the transistor is biased in the saturation region, we have

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$250 = \left(\frac{80}{2}\right) \cdot (3)(V_{GS} - 0.8)^2$$

which yields

$$V_{GS} = 2.24\,\text{V}$$

The voltage at the source terminal is $V_S = -V_{GS} = -2.24\,\text{V}$.

The drain current can also be written as

$$I_D = \frac{5 - V_D}{R_D}$$

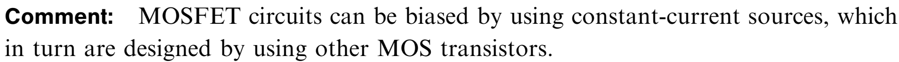
For $V_D = 2.5\,\text{V}$, we have

$$R_D = \frac{5 - 2.5}{0.25} = 10\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_D - V_S = 2.5 - (-2.24) = 4.74\,\text{V}$$

Since $V_{DS} = 4.74\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.44\,\text{V}$, the transistor is biased in the saturation region, as initially assumed.



Comment: MOSFET circuits can be biased by using constant-current sources, which in turn are designed by using other MOS transistors.

Test Your Understanding

RD5.10 For the circuit shown in Figure 5.30(b), the transistor parameters are $V_{TN} = 1.2\,\text{V}$ and $K_n = 0.080\,\text{mA/V}^2$. Redesign the circuit by replacing the current source with a source resistor such that $I_D = 100\,\mu\text{A}$ and $V_{DS} = 4.5\,\text{V}$. (Ans. $R_S = 26.8\,\text{k}\Omega$ and $R_D = 28.2\,\text{k}\Omega$)

D5.11 Consider the circuit shown in Figure 5.31. The transistor parameters are $V_{TP} = -0.8\,\text{V}$ and $K_p = 0.050\,\text{mA/V}^2$. Design the circuit such that $I_D = 120\,\mu\text{A}$ and $V_{SD} = 8\,\text{V}$. (Ans. $R_S = 63.75\,\text{k}\Omega$, $R_D = 36.25\,\text{k}\Omega$)

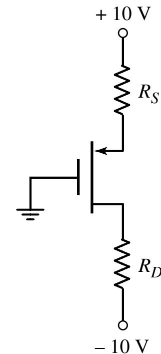


Figure 5.31 Circuit for Exercise 5.11

An enhancement-mode MOSFET connected in a configuration such as that shown in Figure 5.32 can be used as a nonlinear resistor. A transistor with this connection is called an **enhancement load device**. Since the transistor is an enhancement mode device, $V_{TN} > 0$. Also, for this circuit, $v_{DS} = v_{GS} > v_{DS}(\text{sat}) = v_{GS} - V_{TN}$, which means that the transistor is always biased in the saturation region. The general i_D versus v_{DS} characteristics can then be written as

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2 \tag{5.19}$$

Figure 5.33 shows a plot of Equation (5.19) for the case when $K_n = 1\,\text{mA/V}^2$ and $V_{TN} = 1\,\text{V}$.

In the next chapter, we will see how this transistor is used in place of a load resistor in an amplifier circuit. In later chapters, we will show how this transistor is used in digital logic circuits.

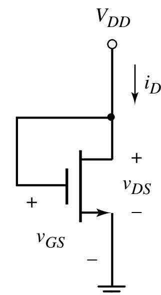


Figure 5.32 Enhancement-mode NMOS device with the gate connected to the drain

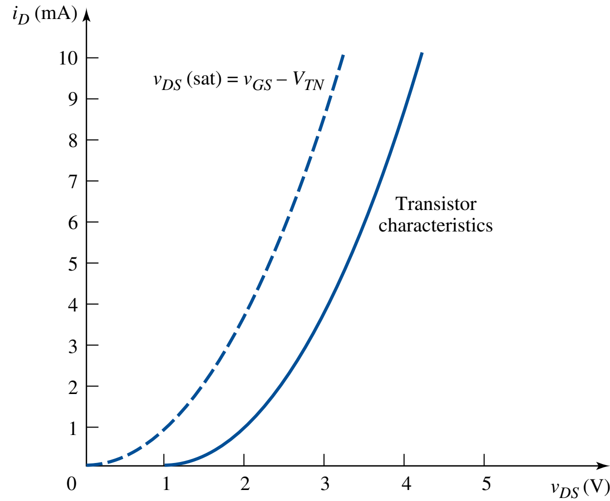


Figure 5.33 Current–voltage characteristic of an enhancement load device

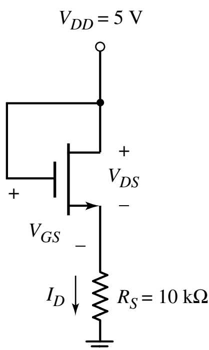


Figure 5.34 Circuit containing an enhancement load device

Example 5.8 **Objective:** Calculate the characteristics of a circuit containing an enhancement load device.

Consider the circuit shown in Figure 5.34 with transistor parameters $V_{TN} = 0.8$ V and $K_n = 0.05$ mA/V^2.

Solution: Since the transistor is biased in the saturation region, the dc drain current is given by

$$I_D = K_n(V_{GS} - V_{TN})^2$$

and the dc drain-to-source voltage is

$$V_{DS} = V_{GS} = 5 - I_D R_S$$

Combining these two equations, we obtain

$$V_{GS} = 5 - K_n R_S (V_{GS} - V_{TN})^2$$

Substituting parameter values, we obtain

$$V_{GS} = 5 - (0.05)(10)(V_{GS} - 0.8)^2$$

which can be written as

$$0.5V_{GS}^2 + 0.2V_{GS} - 4.68 = 0$$

The two possible solutions are

$$V_{GS} = -3.27\text{ V} \quad \text{and} \quad V_{GS} = +2.87\text{ V}$$

Since we are assuming the transistor is conducting, the gate-to-source voltage must be greater than the threshold voltage. We therefore have the following solution:

$$V_{GS} = V_{DS} = 2.87\text{ V} \quad \text{and} \quad I_D = 0.213\text{ mA}$$

Comment: This particular circuit is obviously not an amplifier. However, the transistor connected in this configuration is extremely useful as an effective load resistor.

Test Your Understanding

5.12 The parameters for the circuit shown in Figure 5.34 are changed to $V_{DD} = 10\,\text{V}$ and $R_S = 10\,\text{k}\Omega$, and the transistor parameters are $V_{TN} = 2\,\text{V}$ and $K_n = 0.20\,\text{mA/V}^2$. Calculate I_D, V_{DS}, and the power dissipated in the transistor. (Ans. $V_{GS} = V_{DS} = 3.77\,\text{V}$, $I_D = 0.623\,\text{mA}$, $P = 2.35\,\text{mW}$)

D5.13 The parameters for the circuit shown in Figure 5.34 are $V_{DD} = 5\,\text{V}$ and $R_S = 5\,\text{k}\Omega$. The transistor threshold voltage is $V_{TN} = 1\,\text{V}$. If $k_n' = 40\,\mu\text{A/V}^2$, design the transistor width-to-length ratio such that $V_{DS} = 2.2\,\text{V}$. (Ans. $W/L = 19.5$)

If an enhancement load device is connected in a circuit with another MOSFET in the configuration in Figure 5.35, the circuit can be used as an amplifier or as an inverter in a digital logic circuit. The load device, M_L, is always biased in the saturation region, and the transistor M_D, called the **driver transistor**, can be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. The next example addresses the dc analysis of this circuit for dc input voltages to the gate of M_D.

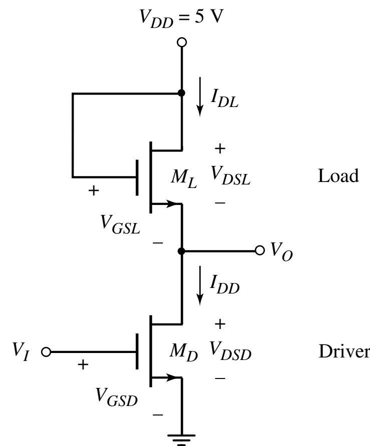


Figure 5.35 Circuit with enhancement load device and NMOS driver

Example 5.9 **Objective:** Determine the dc transistor currents and voltages in a circuit containing an enhancement load device.

The transistors in the circuit shown in Figure 5.35 have parameters $V_{TND} = V_{TNL} = 1\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. (The subscript D applies to the driver transistor and the subscript L applies to the load transistor.) Determine V_O for $V_I = 5\,\text{V}$ and $V_I = 1.5\,\text{V}$.

Solution: ($V_I = 5\,\text{V}$) Assume that the driver transistor M_D is biased in the nonsaturation region. The drain current in the load device is equal to the drain current in the driver transistor. Writing these currents in generic form, we have

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5-1)V_O - V_O^2] = (10)[5 - V_O - 1]^2$$

Rearranging the terms provides

$$3V_O^2 - 24V_O + 8 = 0$$

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.65\,\text{V} \quad \text{or} \quad V_O = 0.349\,\text{V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5\,\text{V}$, the valid solution is $V_O = 0.349\,\text{V}$.

Also, since $V_{DSD} = V_O = 0.349\,\text{V} < V_{GSD} - V_{TND} = 5 - 1 = 4\,\text{V}$, the driver M_D is biased in the nonsaturation region, as initially assumed.

The current can be determined from

$$I_D = K_{nL}(V_{GSL} - V_{TNL})^2 = K_{nL}(V_{DD} - V_O - V_{TNL})^2$$

or

$$I_D = (10)(5 - 0.349 - 1)^2 = 133\,\mu\text{A}$$

Solution: ($V_I = 1.5\,\text{V}$) Assume that the driver transistor M_D is biased in the saturation region. Equating the currents in the two transistors and writing the current equations in generic form, we have

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[V_{GSD} - V_{TND}]^2 = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Again, since $V_{GSD} = V_I$ and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[V_I - V_{TND}]^2 = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers and taking the square root, we find

$$\sqrt{50}[1.5 - 1] = \sqrt{10}[5 - V_O - 1]$$

which yields $V_O = 2.88\,\text{V}$.

Since $V_{DSD} = V_O = 2.88\,\text{V} > V_{GSD} - V_{TND} = 1.5 - 1 = 0.5\,\text{V}$, the driver transistor M_D is biased in the saturation region, as initially assumed.

The current is

$$I_D = K_{nD}(V_{GSD} - V_{TND})^2 = (50)(1.5 - 1)^2 = 12.5\,\mu\text{A}$$

Comment: For this example, we made an initial guess as to whether the driver transistor was biased in the saturation or nonsaturation region. A more analytical approach is shown following this example.

Computer Simulation: The voltage transfer characteristics of the NMOS inverter circuit with the enhancement load shown in Figure 5.35 were obtained by a PSpice analysis. These results are shown in Figure 5.36. For an input voltage less than 1 V, the driver is cut off and the output voltage is $V_O = V_{DD} - V_{TNL} = 5 - 1 = 4\,\text{V}$. As the

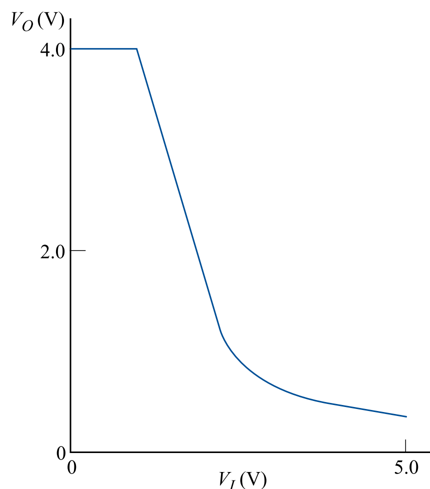


Figure 5.36 Voltage transfer characteristics of NMOS inverter with enhancement load device

input voltage decreases, the output voltage increases, charging and discharging capacitances in the transistors. When the current goes to zero at $V_I = 1$ V and $V_O = 4$ V, the capacitances cease charging and discharging so the output voltage cannot get to the full $V_{DD} = 5$ V value.

When the input voltage is just greater than 1 V, both transistors are biased in the saturation region as the previous analsyis for $V_I = 1.5$ V showed. The output voltage is a linear function of input voltage.

For an input voltage greater than approximately 2.25 V, the driver transistor is biased in the nonsaturation region and the output voltage is a nonlinear function of the input voltage.

In the circuit shown in Figure 5.35, we can determine the transition point for the driver transistor that separates the saturation and nonsaturation regions. The transition point is determined by the equation

$$V_{DSD}(\text{sat}) = V_{GSD} - V_{TND} \tag{5.20}$$

Again, the drain currents in the two transistors are equal. Using the saturation drain current relationship for the driver transistor, we have

$$I_{DD} = I_{DL} \tag{5.21(a)}$$

or

$$K_{nD}[V_{GSD} - V_{TND}]^2 = K_{nL}[V_{GSL} - V_{TNL}]^2 \tag{5.21(b)}$$

Again, noting that $V_{GSD} = V_I$ and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, and taking the square root, we have

$$\sqrt{\frac{K_{nD}}{K_{nL}}}(V_I - V_{TND}) = (V_{DD} - V_O - V_{TNL}) \tag{5.22}$$

At the transition point, we can define the input voltage as $V_I = V_{It}$ and the output voltage as $V_{Ot} = V_{DSD}(\text{sat}) = V_{It} - V_{TND}$. Then, from Equation (5.22), the input voltage at the transition point is

$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}(1 + \sqrt{K_{nD}/K_{NL}})}{1 + \sqrt{K_{nD}/K_{nL}}} \tag{5.23}$$

If we apply Equation (5.23) to the previous example, we can show that our initial assumptions were correct.

Test Your Understanding

5.14 For the circuit shown in Figure 5.35, use the transistor parameters given in Example 5.9. (a) Determine V_I and V_O at the transition point for the driver transistor. (b) Calculate the transistor currents at the transition point. (Ans. (a) $V_{It} = 2.24\,\text{V}$, $V_{Ot} = 1.24\,\text{V}$; (b) $I_D = 76.9\,\mu\text{A}$)

D5.15 Consider the circuit shown in Figure 5.35 with transistor parameters $V_{TND} = V_{TNL} = 1\,\text{V}$. (a) Design the ratio K_{nD}/K_{nL} that will produce a transition point at $V_I = 2.5\,\text{V}$. (b) Using the results of part (a), find V_O for $V_I = 5\,\text{V}$. (Ans. (a) $K_{nD}/K_{nL} = 2.78$ (b) $V_O = 0.57\,\text{V}$)

Up to this point, we have only considered the n-channel enhancement-mode MOSFET as a load device. An n-channel depletion-mode MOSFET can also be used. Consider the depletion-mode MOSFET with the gate and source connected together shown in Figure 5.37(a). The current–voltage characteristics are shown in Figure 5.37(b). The transistor may be biased in either the saturation or nonsaturation regions. The transition point is also shown on the plot. The threshold voltage of the n-channel depletion-mode MOSFET is negative so that $v_{DS}(\text{sat})$ is positive.

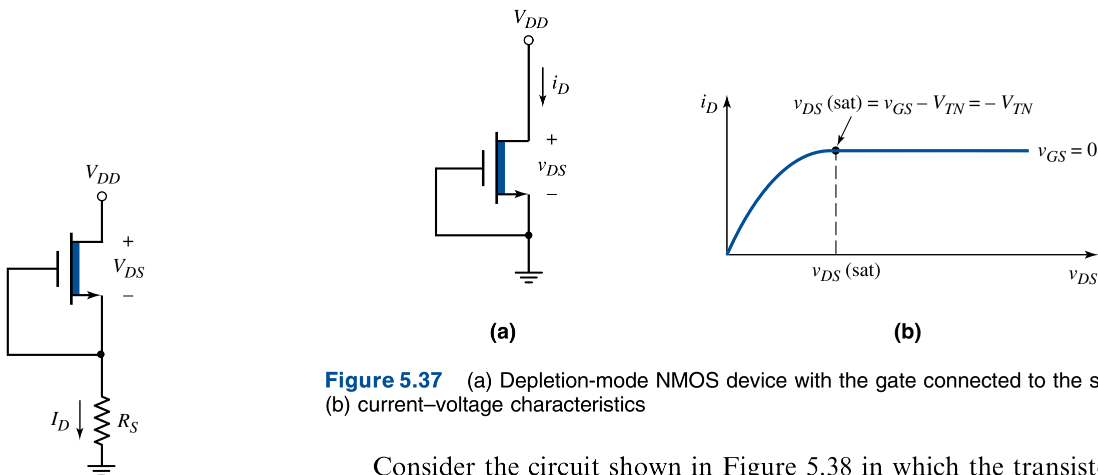


Figure 5.37 (a) Depletion-mode NMOS device with the gate connected to the source and (b) current–voltage characteristics

Figure 5.38 Circuit containing a depletion load device

Consider the circuit shown in Figure 5.38 in which the transistor is being used as a **depletion load device**. It may be biased in the saturation or nonsaturation region, depending on the values of the transistor parameters and V_{DD} and R_S.

Example 5.10 **Objective:** Calculate the characteristics of a circuit containing a depletion load device.

For the circuit shown in Figure 5.38 the transistor parameters are $V_{TN} = -2\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$. Assume that $V_{DD} = 5\,\text{V}$ and $R_S = 5\,\text{k}\Omega$.

Solution: If we assume that the transistor is biased in the saturation region, then the dc drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = K_n(-V_{TN})^2 = (0.1)(-(-2))^2 = 0.4\,\text{mA}$$

In this case, the transistor is acting as a constant-current source. The dc drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_S = 5 - (0.4)(5) = 3\,\text{V}$$

Since

$$V_{DS} = 3\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 0 - (-2) = 2\,\text{V}$$

the transistor is biased in the saturation region.

Comment: Although this circuit is also not an amplifier, this transistor configuration is useful as an effective load resistor in both analog and digital circuits.

Test Your Understanding

5.16 For the circuit shown in Figure 5.38, the circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_S = 4\,\text{k}\Omega$, and the transistor parameters are $V_{TN} = -2.5\,\text{V}$ and $K_n = 0.25\,\text{mA/V}^2$. Calculate I_D, V_{DS}, and the power dissipated in the transistor. Is the transistor biased in the saturation or nonsaturation region? (Ans. $I_D = 1.56\,\text{mA}$, $V_{DS} = 3.76\,\text{V}$, $P = 5.87\,\text{mW}$, saturation region)

D5.17 The parameters for the circuit shown in Figure 5.38 are $V_{DD} = 5\,\text{V}$ and $R_S = 8\,\text{k}\Omega$. The transistor threshold voltage is $V_{TN} = -1.8\,\text{V}$. If $k_n' = 35\,\mu\text{A/V}^2$, design the transistor width-to-length ratio such that $V_{DS} = 1.2\,\text{V}$. Is the transistor biased in the saturation or nonsaturation region? (Ans. $W/L = 9.43$, nonsaturation)

A depletion load device can be used in conjunction with another MOSFET, as shown in Figure 5.39, to create a circuit that can be used as an amplifier or as an inverter in a digital logic circuit. Both the load device M_L and driver transistor M_D may be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. We will perform the dc analysis of this circuit for a particular dc input voltage to the gate of the driver transistor.

Example 5.11 **Objective:** Determine the dc transistor currents and voltages in a circuit containing a depletion load device.

Consider the circuit shown in Figure 5.39 with transistor parameters: $V_{TND} = 1\,\text{V}$, $V_{TNL} = -2\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. Determine V_O for $V_I = 5\,\text{V}$.

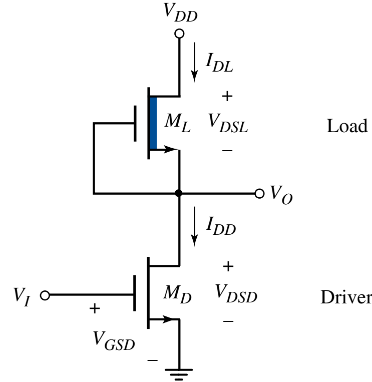


Figure 5.39 Circuit with depletion load device and NMOS driver

Solution: Assume the driver transistor M_D is biased in the nonsaturation region and the load transistor M_L is biased in the saturation region. The drain currents in the two transistors are equal. In generic form, these currents are

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = 0$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[-V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5-1)V_O - V_O^2] = (10)[-(-2)]^2$$

Rearranging the terms produces

$$5V_O^2 - 40V + 4 = 0$$

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.90\text{ V} \quad \text{or} \quad V_O = 0.10\text{ V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5$ V, the valid solution is $V_O = 0.10$ V.

The current is

$$I_D = K_{nL}(-V_{TNL})^2 = (10)[-(-2)]^2 = 40\ \mu\text{A}$$

Comment: Since $V_{DSD} = V_O = 0.10\text{ V} < V_{GSD} - V_{TND} = 5 - 1 = 4$ V, M_D is biased in the nonsaturation region, as assumed. Similarly, since $V_{DSL} = V_{DD} - V_O = 4.9\text{ V} > V_{GSL} - V_{TNL} = 0 - (-2) = 2$ V, M_L is biased in the saturation region, as originally assumed.

Computer Simulation: The voltage transfer characteristics of the NMOS inverter circuit with depletion load in Figure 5.39 were obtained using a PSpice analysis. These results are shown in Figure 5.40. For an input voltage less than 1 V, the driver is cut off and the output voltage is $V_O = V_{DD} = 5$ V.

When the input voltage is just greater than 1 V, the driver transistor is biased in the saturation region and the load device in the nonsaturation region. When the input voltage is approximately 1.9 V, both transistors are biased in the saturation region. If

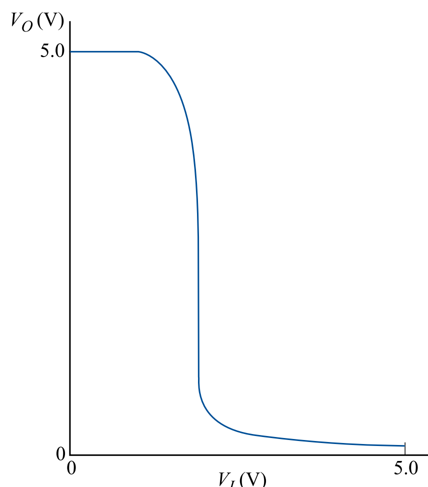


Figure 5.40 Voltage transfer characteristics of NMOS inverter with depletion load device

the channel length modulation parameter λ is assumed to be zero as in this example, there is no change in the input voltage during this transition region. As the input voltage becomes larger than 1.9 V, the driver is biased in the nonsaturation region and the load in the saturation region.

Test Your Understanding

5.18 For the circuit shown in Figure 5.39, use the transistor parameters given in Example 5.11. (a) Determine V_I and V_O at the transition point for the load transistor. (b) Determine V_I and V_O at the transition point for the driver transistor. (Ans. (a) $V_{It} = 1.89\,\text{V}$, $V_{Ot} = 3\,\text{V}$; (b) $V_{It} = 1.89\,\text{V}$, $V_{Ot} = 0.89\,\text{V}$)

D5.19 Consider the circuit shown in Figure 5.39 with transistor parameters $V_{TND} = 1\,\text{V}$ and $V_{TNL} = -2\,\text{V}$. (a) Design the ratio K_{nD}/K_{nL} that will produce an output voltage of $V_O = 0.25\,\text{V}$ at $V_I = 5\,\text{V}$. (b) Find K_{nD} and K_{nL} if the transistor currents are 0.2 mA when $V_I = 5\,\text{V}$. (Ans. (a) $K_{nD}/K_{nL} = 2.06$ (b) $K_{nL} = 50\,\mu\text{A/V}^2$, $K_{nD} = 103\,\mu\text{A/V}^2$)

A p-channel enhancement-mode transistor can also be used as a load device to form a **complementary MOS (CMOS)** inverter. The term complementary implies that both n-channel and p-channel transistors are used in the same circuit. The CMOS technology is used extensively in both analog and digital electronic circuits.

Figure 5.41 shows one example of a CMOS inverter. The NMOS transistor is used as the amplifying device, or the driver, and the PMOS device is the load, which is referred to as an active load. This configuration is typically used in analog applications. In another configuration, the two gates are tied together and forms the input. This configuration will be discussed in detail in Chapter 16.

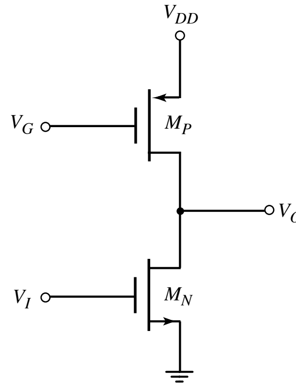


Figure 5.41 Example of CMOS inverter

As with the previous two NMOS inverters, the two transistors shown in Figure 5.41 may be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. The voltage transfer characteristic is most easily determined from a PSpice analysis.

Example 5.12 **Objective:** Determine the voltage transfer characteristic of the CMOS inverter using a PSpice analysis.

For the circuit shown in Figure 5.41, assume transistor parameters of $V_{TN} = 1\,\text{V}$, $V_{TP} = -1\,\text{V}$, and $K_n = K_p$. Also assume $V_{DD} = 5\,\text{V}$ and $V_G = 3.25\,\text{V}$.

Solution: The voltage transfer characteristics are shown in Figure 5.42. In this case, there is a region, as was the case for an NMOS inverter with depletion load, in which both transistors are biased in the saturation region, and the input voltage is a constant over this transition region for the assumption that the channel length modulation parameter λ is zero.

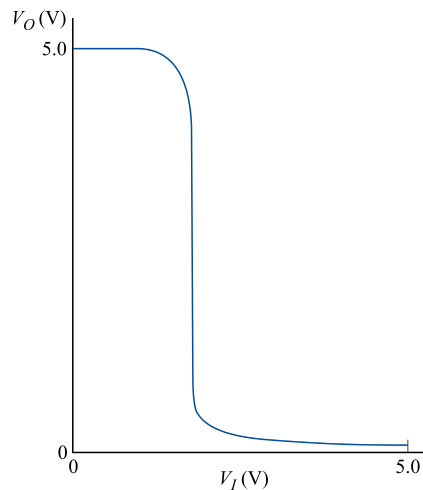


Figure 5.42 Voltage transfer characteristics of CMOS inverter in Figure 5.41

Comment: In this example, the source-to-gate voltage of the PMOS device is only $V_{SG} = 0.75$ V. The effective resistance looking into the drain of the PMOS device is then relatively large. This is a desirable characteristic for an amplifier, as we will see in the next chapter.

5.2.4 Constant-Current Source Biasing

As was shown in Figure 5.30, a MOSFET can be biased by using a constant-current source I_Q. The advantage of this circuit is that the drain current is independent of the transistor parameters.

The constant-current source can be implemented by using MOSFETs as shown in Figure 5.43. The transistors M_2, M_3, and M_4 form the current source. Transistors M_3 and M_4 are each connected in a diode-type configuration, and they establish a reference current. We noted in the last section that this diode-type connection implies the transistor is always biased in the saturation region. Transistors M_3 and M_4 are therefore biased in the saturation region, and M_2 is assumed to be biased in the saturation region. The resulting gate-to-source voltage on M_3 is applied to M_2, and this establishes the bias current I_Q.

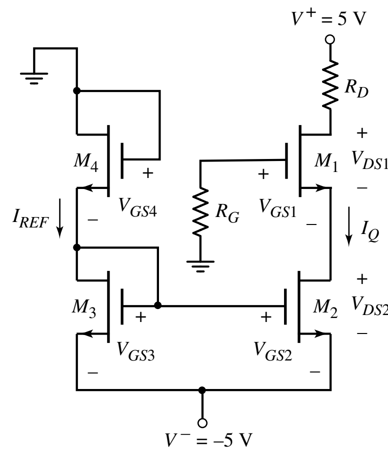


Figure 5.43 Implementation of a MOSFET constant-current source

Since the reference current is the same in transistors M_3 and M_4, we can write

$$K_{n3}(V_{GS3} - V_{TN3})^2 = K_{n4}(V_{GS4} - V_{TN4})^2 \quad \textbf{(5.24)}$$

We also know that

$$V_{GS4} + V_{GS3} = (-V^-) \quad \textbf{(5.25)}$$

Solving Equation (5.25) for V_{GS4} and substituting the result into Equation (5.24) yields

$$V_{GS3} = \frac{\sqrt{\frac{K_{n4}}{K_{n3}}}[(-V^-) - V_{TN4}] + V_{TN3}}{1 + \sqrt{\frac{K_{n4}}{K_{n3}}}} \quad \textbf{(5.26)}$$

Since $V_{GS3} = V_{GS2}$, the bias current is

$$I_Q = K_{n2}(V_{GS3} - V_{TN2})^2 \quad \textbf{(5.27)}$$

Example 5.13 **Objective:** Determine the currents and voltages in a MOSFET constant-current source.

For the circuit shown in Figure 5.43, the transistor parameters are: $K_{n1} = 0.2\,\text{mA/V}^2$, $K_{n2} = K_{n3} = K_{n4} = 0.1\,\text{mA/V}^2$, and $V_{TN1} = V_{TN2} = V_{TN3} = V_{TN4} = 1\,\text{V}$.

Solution: From Equation (5.26), we can determine V_{GS3}, as follows:

$$V_{GS3} = \frac{\sqrt{\frac{0.1}{0.1}}[5 - 1] + 1}{1 + \sqrt{\frac{0.1}{0.1}}} = 2.5\,\text{V}$$

Since M_3 and M_4 are identical transistors, V_{GS3} should be one-half of the bias voltage. The bias current I_Q is then

$$I_Q = (0.1) \cdot (2.5 - 1)^2 = 0.225\,\text{mA}$$

The gate-to-source voltage on M_1 is found from

$$I_Q = K_{n1}(V_{GS1} - V_{TN1})^2$$

or

$$0.225 = (0.2) \cdot (V_{GS1} - 1)^2$$

which yields

$$V_{GS1} = 2.06\,\text{V}$$

The drain-to-source voltage on M_2 is

$$V_{DS2} = (-V^-) - V_{GS1} = 5 - 2.06 = 2.94\,\text{V}$$

Since $V_{DS2} = 2.94\,\text{V} > V_{DS}(\text{sat}) = V_{GS2} - V_{TN2} = 2.5 - 1 = 1.5\,\text{V}$, M_2 is biased in the saturation region.

Design Consideration: Since in this example M_2 and M_3 are identical transistors, the reference current I_{REF} and bias current I_Q are equal. By redesigning the width-to-length ratios of M_2, M_3, and M_4, we can obtain a specific bias current I_Q. If M_2 and M_3 are not identical, then I_Q and I_{REF} will not be equal. A variety of design options are possible with such a circuit configuration.

Test Your Understanding

D5.20 Consider the constant-current source shown in Figure 5.43. Assume that the threshold voltage of each transistor is $V_{TN} = 1\,\text{V}$. (a) Design the ratio of K_{n4}/K_{n3} such that $V_{GS3} = 2\,\text{V}$. (b) Determine K_{n2} such that $I_Q = 100\,\mu\text{A}$. (c) Find K_{n3} and K_{n4} such that $I_{REF} = 200\,\mu\text{A}$. (Ans. (a) $K_{n4}/K_{n3} = \frac{1}{4}$ (b) $K_{n2} = 0.1\,\text{mA/V}^2$ (c) $K_{n3} = 0.2\,\text{mA/V}^2$, $K_{n4} = 0.05\,\text{mA/V}^2$)

5.3 BASIC MOSFET APPLICATIONS: SWITCH, DIGITAL LOGIC GATE, AND AMPLIFIER

MOSFETs may be used to: switch currents, voltages, and power; perform digital logic functions; and amplify small time-varying signals. In this section, we will examine the switching properties of an NMOS transistor, analyze a simple NMOS transistor digital logic circuit, and discuss how the MOSFET can be used to amplify small signals.

5.3.1 NMOS Inverter

The MOSFET can be used as a switch in a wide variety of electronic applications. The transistor switch provides an advantage over mechanical switches in both speed and reliability. The transistor switch considered in this section is also called an inverter. Two other switch configurations, the NMOS transmission gate and the CMOS transmission gate, are discussed in Chapter 16.

Figure 5.44 shows the n-channel enhancement-mode MOSFET inverter circuit. If $v_I < V_{TN}$, the transistor is in cutoff and $i_D = 0$. There is no voltage drop across R_D, and the output voltage is $v_O = V_{DD}$. Also, since $i_D = 0$, no power is dissipated in the transistor.

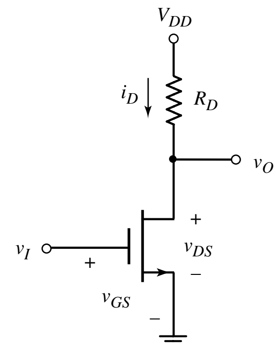


Figure 5.44 NMOS inverter circuit

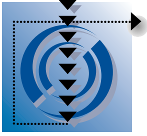
If $v_I > V_{TN}$, the transistor is on and initially is biased in the saturation region, since $v_{DS} > v_{GS} - V_{TN}$. As the input voltage increases, the drain-to-source voltage decreases, and the transistor eventually becomes biased in the nonsaturation region. When $v_I = V_{DD}$, the transistor is biased in the nonsaturation region, v_O reaches a minimum value, and the drain current reaches a maximum value. The current and voltage are given by

$$i_D = K_n[2(v_I - V_{TN})v_O - v_O^2] \tag{5.28}$$

and

$$v_O = v_{DD} - i_D R_D \tag{5.29}$$

where $v_O = v_{DS}$ and $v_I = v_{GS}$.



Design Example 5.14 **Objective:** Design the size of a power MOSFET to meet the specification of a particular switch application.

The load in the inverter circuit in Figure 5.44 is a coil of an electromagnet that requires a current of 0.5 A when turned on. The effective load resistance varies between 8 and 10 Ω, depending on temperature and other variables. A 10 V power supply is available. The transistor parameters are $k_n' = 80\,\mu\text{A/V}^2$ and $V_{TN} = 1\,\text{V}$.

Solution: One solution is to bias the transistor in the saturation region so that the current is constant, independent of the load resistance.

The minimum V_{DS} value is 5 V. We need $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$. If we bias the transistor at $V_{GS} = 5\,\text{V}$, then the transistor will always be biased in the saturation region. We can then write

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$0.5 = \frac{80 \times 10^{-6}}{2}\left(\frac{W}{L}\right) \cdot (5-1)^2$$

which yields $W/L = 781$.

The maximum power dissipated in the transistor is

$$P(\text{max}) = V_{DS}(\text{max}) \cdot I_D = (6) \cdot (0.5) = 3\,\text{W}$$

Comment: We see that we can switch a relatively large drain current with essentially no input current to the transistor. The size of the transistor required is fairly large, which implies a power transistor is necessary. If a transistor with a slightly different width-to-length ratio is available, the applied V_{GS} can be changed to meet the specification.

Test Your Understanding

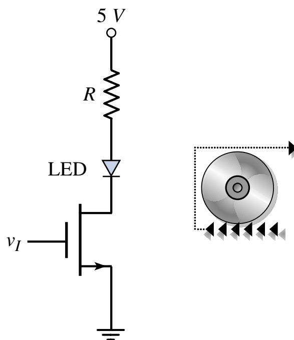


Figure 5.45

5.21 For the MOS inverter circuit shown in Figure 5.44, assume the circuit values are: $V_{DD} = 5\,\text{V}$ and $R_D = 10\,\text{k}\Omega$. The threshold voltage of the transistor is $V_{TN} = 1\,\text{V}$. Determine the value of the conduction parameter K_n such that $v_O = 1\,\text{V}$ when $v_I = 5\,\text{V}$. What is the power dissipated in the transistor? (Ans. $K_n = 0.057\,\text{mA/V}^2$, $P = 0.4\,\text{mW}$)

D5.22 The circuit shown in Figure 5.44 is biased with $V_{DD} = 10\,\text{V}$ and the transistor has parameters $V_{TN} = 0.70\,\text{V}$ and $K_n = 0.050\,\text{mA/V}^2$. Design the value of R_D for which the output voltage will be $v_O = 0.35\,\text{V}$, when $v_I = 10\,\text{V}$. (Ans. $R_D = 30.3\,\text{k}\Omega$)

D5.23 The transistor in the circuit shown in Figure 5.45 has parameters $K_n = 4\,\text{mA/V}^2$ and $V_{TN} = 0.8\,\text{V}$, and is used to switch the LED on and off. The LED cutin voltage is $V_\gamma = 1.5\,\text{V}$. The LED is turned on by applying an input voltage of $v_I = 5\,\text{V}$. (a) Determine the value of R such that the diode current is 12 mA. (b) From the results of part (a), what is the value of v_{DS}? (Ans. (a) $R = 261\,\Omega$, (b) $v_{DS} = 0.374\,\text{V}$)

5.3.2 Digital Logic Gate

For the transistor inverter circuit in Figure 5.44, when the input is low and approximately zero volts, the transistor is cut off, and the output is high and equal to V_{DD}. When the input is high and equal to V_{DD}, the transistor is biased in the nonsaturation region and the output reaches a low value. Since the input voltages will be either high or low, we can analyze the circuit in terms of dc parameters.

Now consider the case when a second transistor is connected in parallel, as shown in Figure 5.46. If the two inputs are zero, both M_1 and M_2 are cut off, and $V_O = 5\,\text{V}$. When $V_1 = 5\,\text{V}$ and $V_2 = 0$, the transistor M_1 turns on and M_2 is still cut off. Transistor M_1 is biased in the nonsaturation region, and V_O reaches a low value. If we reverse the input voltages such that $V_1 = 0$ and $V_2 = 5\,\text{V}$, then M_1 is cut off and M_2 is biased in the nonsaturation region. Again, V_O is at a low value. If both inputs are high, at $V_1 = V_2 = 5\,\text{V}$, then both transistors are biased in the nonsaturation region and V_O is low.

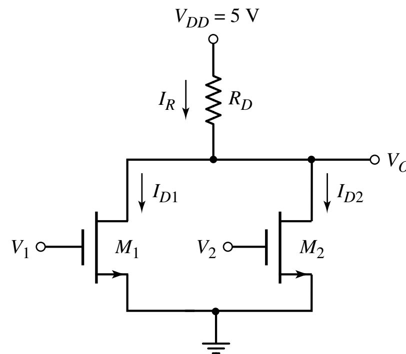


Figure 5.46 A two-input NMOS NOR logic gate

Table 5.2 shows these various conditions for the circuit in Figure 5.46. In a positive logic system, these results indicate that this circuit performs the NOR logic function, and, it is therefore called a two-input NOR logic circuit. In actual NMOS logic circuits, the resistor R_D is replaced by another NMOS transistor.

Table 5.2 NMOS NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

Objective: Determine the currents and voltages in a digital logic gate, for various input conditions.

Consider the circuit shown in Figure 5.46 with circuit and transistor parameters $R_D = 20\,\text{k}\Omega$, $K_n = 0.1\,\text{mA/V}^2$, and $V_{TN} = 0.8\,\text{V}$.

Solution: For $V_1 = V_2 = 0$, both M_1 and M_2 are cut off and $V_O = V_{DD} = 5\,\text{V}$. For $V_1 = 5\,\text{V}$ and $V_2 = 0$, the transistor M_1 is biased in the nonsaturation region, and we can write

$$I_R = I_{D1} = \frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2]$$

Solving for the output voltage V_O, we obtain $V_O = 0.29\,\text{V}$.

The currents are

$$I_R = I_{D1} = \frac{5 - 0.29}{20} = 0.236\,\text{mA}$$

For $V_1 = 0$ and $V_2 = 5\,\text{V}$, we have $V_O = 0.29\,\text{V}$ and $I_R = I_{D2} = 0.236\,\text{mA}$. When both inputs go high to $V_1 = V_2 = 5\,\text{V}$, we have $I_R = I_{D1} + I_{D2}$, or

$$\frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2] + K_n[2(V_2 - V_{TN})V_O - V_O^2]$$

which can be solved for V_O to yield $V_O = 0.147\,\text{V}$.

The currents are

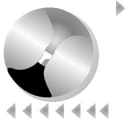
$$I_R = \frac{5 - 0.147}{20} = 0.243\,\text{mA}$$

and

$$I_{D1} = I_{D2} = \frac{I_R}{2} = 0.121\,\text{mA}$$

Comment: When either transistor is biased on, it is biased in the nonsaturation region, since $V_{DS} < V_{DS}(\text{sat})$, and the output voltage reaches a low state.

This example and discussion illustrates that MOS transistors can be configured in a circuit to perform logic functions. A more detailed analysis and design of MOSFET logic gates and circuits is presented in Chapter 16.



5.24 For the circuit in Figure 5.46, assume the circuit and transistor parameters are: $R_D = 30\,\text{k}\Omega$, $V_{TN} = 1\,\text{V}$, and $K_n = 50\,\mu\text{A/V}^2$. Determine V_O, I_R, I_{D1}, and I_{D2} for: (a) $V_1 = 5\,\text{V}$, $V_2 = 0$; and (b) $V_1 = V_2 = 5\,\text{V}$. (Ans. (a) $V_O = 0.40\,\text{V}$, $I_R = I_{D1} = 0.153\,\text{mA}$, $I_{D2} = 0$ (b) $V_O = 0.205\,\text{V}$, $I_R = 0.16\,\text{mA}$, $I_{D1} = I_{D2} = 0.080\,\text{mA}$)

5.25 In the circuit in Figure 5.46, let $R_D = 25\,\text{k}\Omega$ and $V_{TN} = 1\,\text{V}$. (a) Determine the value of the conduction parameter K_n required such that $V_O = 0.10\,\text{V}$ when $V_1 = 0$ and $V_2 = 5\,\text{V}$. (b) Using the results of part (a), find the value of V_O when $V_1 = V_2 = 5\,\text{V}$. (Ans. (a) $K_n = 0.248\,\text{mA/V}^2$, (b) $V_O = 0.0502\,\text{V}$)

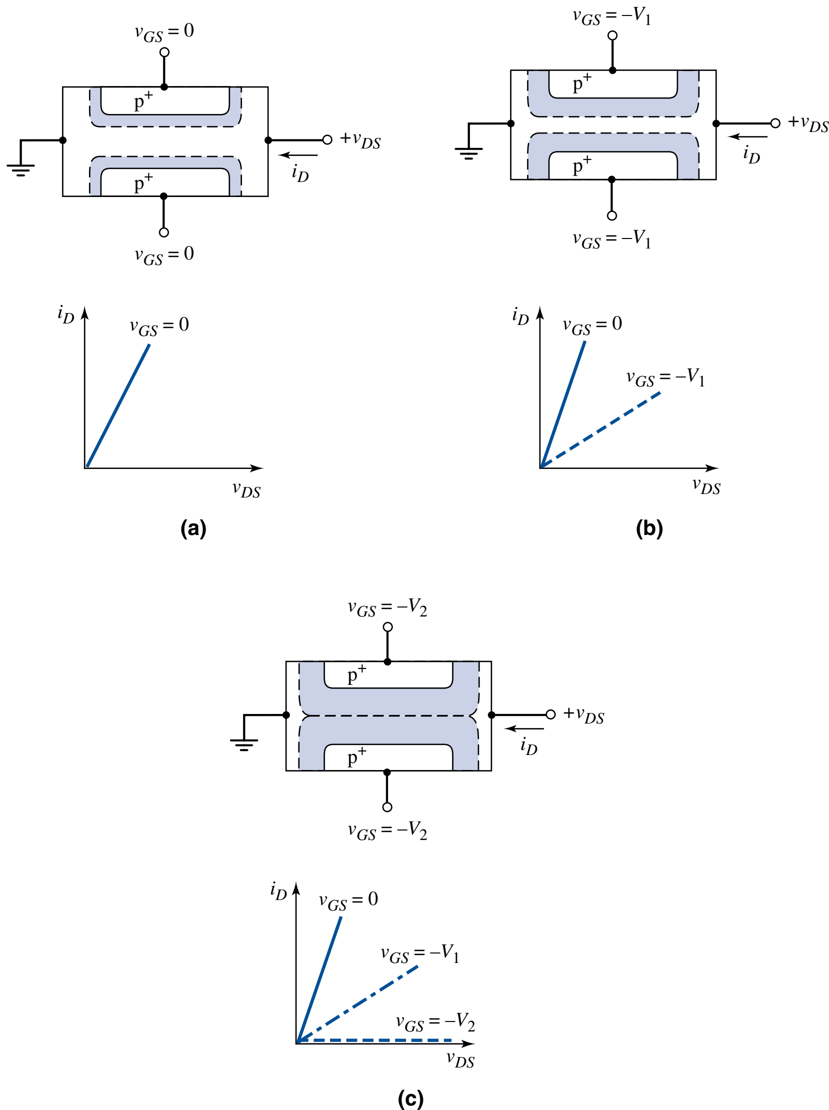


Figure 5.49 Gate-to-channel space-charge regions and current–voltage characteristics for small drain-to-source voltages and for: (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage that achieves pinchoff

n-channel increases, and the slope of the i_D versus v_{DS} curve, for small v_{DS}, decreases. These effects are shown in Figure 5.49(b). If a larger negative gate voltage is applied, the condition shown in Figure 5.49(c) can be achieved. The reverse-biased gate-to-channel space-charge region completely fills the channel region. This condition is known as **pinchoff**. Since the depletion region isolates the source and drain terminals, the drain current at pinchoff is essentially zero. The i_D versus v_{DS} curves are shown in Figure 5.49(c). The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. The pn JFET is a ''normally on,'' or depletion mode, device; that is, a voltage must be applied to the gate terminal to turn the device off.

Consider the situation in which the gate voltage is zero, $v_{GS} = 0$, and the drain voltage changes, as shown in Figure 5.50(a). As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse biased near the drain terminal, and the space-charge region widens, extending farther into the channel. The channel acts essentially as a resistor, and the effective channel resistance increases as the space-charge region widens; therefore, the slope of the i_D versus v_{DS} characteristic decreases, as shown in Figure 5.50(b). The effective channel resistance now varies along the channel length, and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

If the drain voltage increases further, the condition shown in Figure 5.50(c) can result. The channel is pinched off at the drain terminal. Any

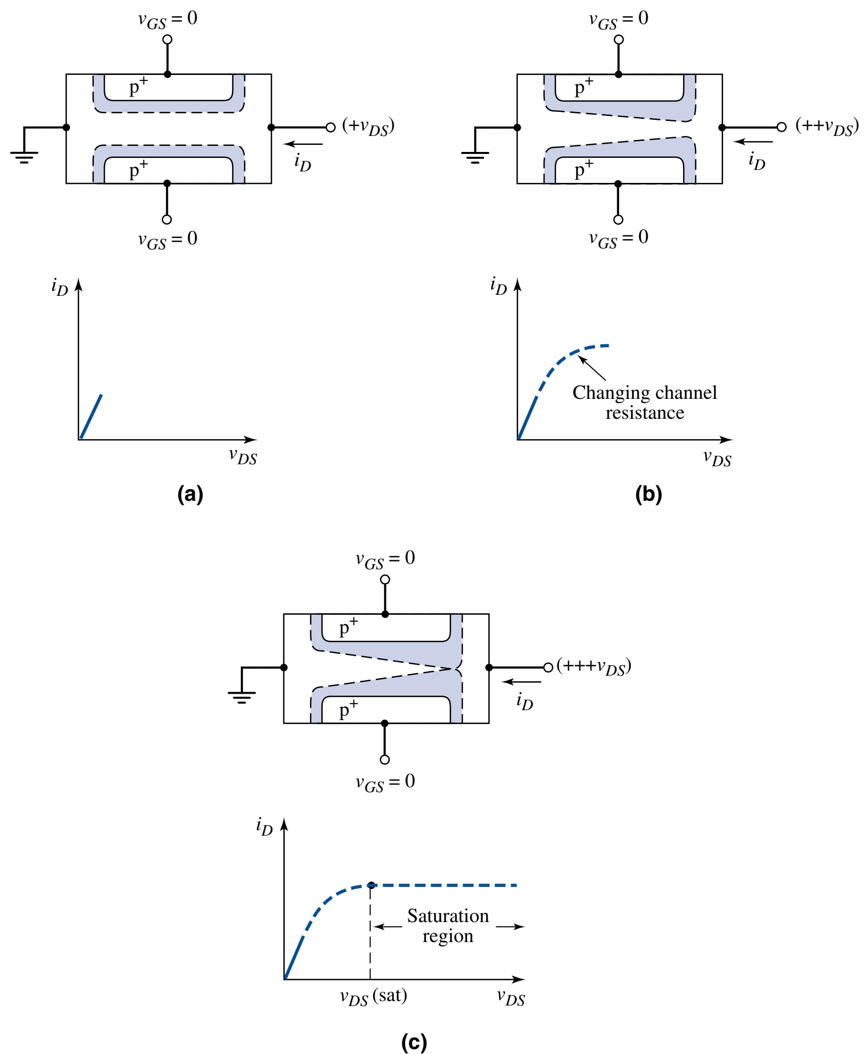


Figure 5.50 Gate-to-channel space-charge regions and current–voltage characteristics for zero gate voltage and for: (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage that achieves pinchoff at the drain terminal

further increase in drain voltage will not increase the drain current. The i_D–v_{DS} characteristic for this condition is also shown in the figure. The drain voltage at pinchoff is $v_{DS}(\text{sat})$. Therefore, for $v_{DS} > v_{DS}(\text{sat})$, the transistor is biased in the saturation region, and the drain current for this ideal case is independent of v_{DS}.

MESFET

In the MESFET, the gate junction is a Schottky barrier junction, instead of a pn junction. Although MESFETs can be fabricated in silicon, they are usually associated with gallium arsenide or other compound-semiconductor materials.

A simplified cross section of a GaAs MESFET is shown in Figure 5.51. A thin, epitaxial layer of GaAs is used for the active region; the substrate is a very high resistivity GaAs material, referred to as a semi-insulating substrate. The advantages of these devices include: higher electron mobility in GaAs, hence smaller transit time and faster response; and decreased parasitic capacitance and a simplified fabrication process, resulting from the semi-insulating GaAs substrate.

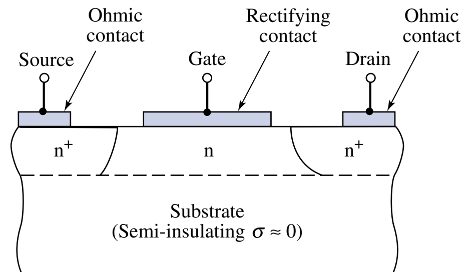


Figure 5.51 Cross section of an n-channel MESFET with a semi-insulating substrate

In the MESFET in Figure 5.51, a reverse-bias gate-to-source voltage induces a space-charge region under the metal gate, which modulates the channel conductance, as in the case of the pn JFET. If a negative applied gate voltage is sufficiently large, the space-charge region will eventually reach the substrate. Again, pinchoff will occur. Also, the device shown in the figure is a depletion mode device, since a gate voltage must be applied to pinch off the channel, that is, to turn the device off.

In another type of MESFET, the channel is pinched off even at $v_{GS} = 0$, as shown in Figure 5.52(a). For this MESFET, the channel thickness is smaller than the zero-biased space-charge width. To open a channel, the depletion region must be reduced; that is, a forward-biased voltage must be applied to the gate–semiconductor junction. When a slightly forward-bias voltage is applied, the depletion region extends just to the width of the channel as shown in Figure 5.52(b). The threshold voltage is the gate-to-source voltage required to create the pinchoff condition. The threshold voltage for this n-channel MESFET is positive, in contrast to the negative threshold voltage of the n-channel depletion-mode device. If a larger forward-bias voltage is applied, the channel region opens, as shown in Figure 5.52(c). The applied

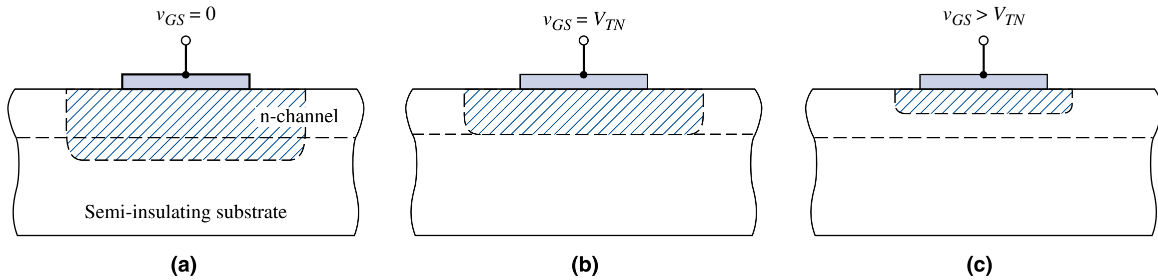


Figure 5.52 Channel space-charge region of an enhancement-mode MESFET for: (a) $v_{GS} = 0$, (b) $v_{GS} = V_{TN}$, and (c) $v_{GS} > V_{TN}$

forward-bias gate voltage is limited to a few tenths of a volt before a significant gate current occurs.

This device is an **n-channel enhancement-mode MESFET**. Enhancement-mode p-channel MESFETs and enhancement-mode pn JFETs have also been fabricated. The advantage of enhancement-mode MESFETs is that circuits can be designed in which the voltage polarities on the gate and drain are the same. However, the output voltage swing of these devices is quite small.

5.4.2 Current–Voltage Characteristics

The circuit symbols for the n-channel and p-channel JFETs are shown in Figure 5.53, along with the gate-to-source voltages and current directions. The ideal current–voltage characteristics, when the transistor is biased in the saturation region, are described by

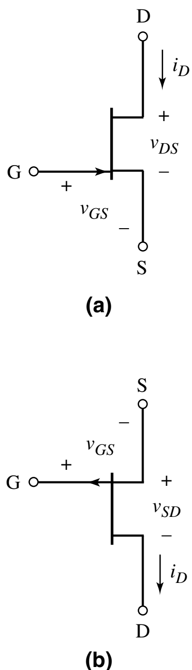


Figure 5.53 Circuit symbols for: (a) n-channel JFET and (b) p-channel JFET

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \quad \textbf{(5.30)}$$

where I_{DSS} is the saturation current when $v_{GS} = 0$, and V_P is the **pinchoff voltage**.

The current–voltage characteristics for n-channel and p-channel JFETs are shown in Figures 5.54(a) and 5.54(b), respectively. Note that the pinchoff voltage V_P for the n-channel JFET is negative and the gate-to-source voltage v_{GS} is usually negative; therefore, the ratio v_{GS}/V_P is positive. Similarly, the pinchoff voltage V_P for the p-channel JFET is positive and the gate-to-source voltage v_{GS} must be positive, and therefore the ratio v_{GS}/V_P is positive.

For the n-channel device, the saturation region occurs when $v_{DS} \geq v_{DS}(\text{sat})$ where

$$v_{DS}(\text{sat}) = v_{GS} - V_P \quad \textbf{(5.31)}$$

For the p-channel device, the saturation region occurs when $v_{SD} \geq v_{SD}(\text{sat})$ where

$$v_{SD}(\text{sat}) = V_P - v_{GS} \quad \textbf{(5.32)}$$

The voltage transfer characteristics of i_D versus v_{GS}, when the transistor is biased in the saturation region, are shown in Figure 5.55, for both the n-channel and p-channel JFET.

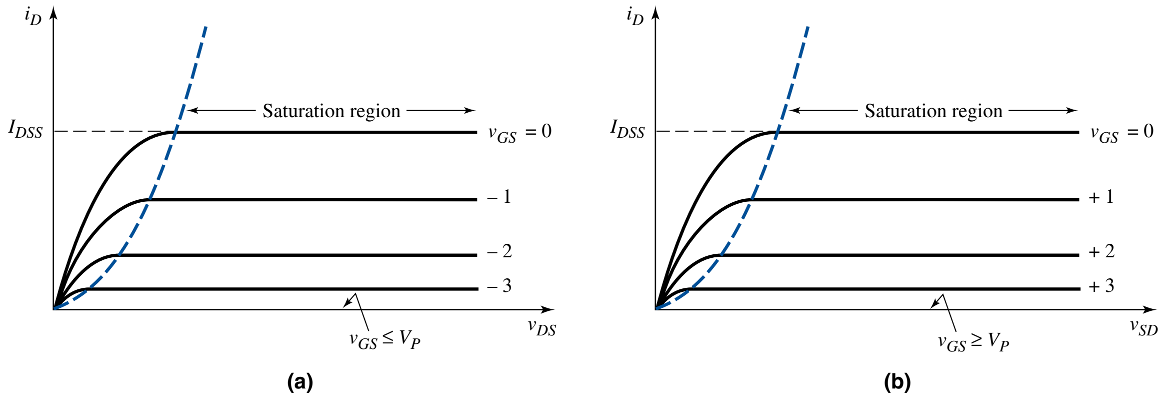


Figure 5.54 Current–voltage characteristics for: (a) n-channel JFET and (b) p-channel JFET

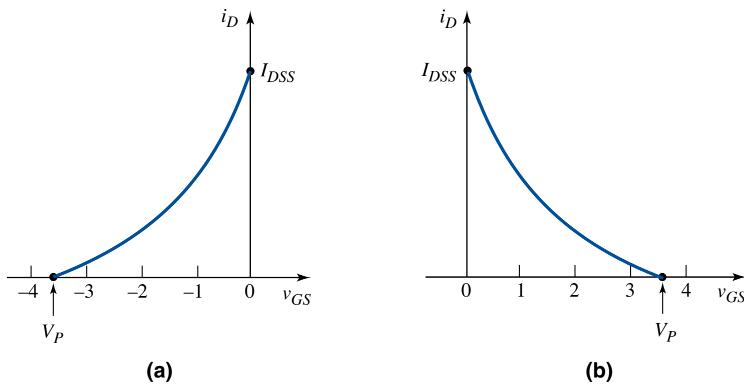


Figure 5.55 Drain current versus gate-to-source voltage characteristics for the transistor biased in the saturation region (a) n-channel JFET and (b) p-channel JFET.

Example 5.16 **Objective:** Calculate i_D and $v_{DS}(\text{sat})$ in an n-channel pn JFET.

Assume the saturation current is $I_{DSS} = 2\,\text{mA}$ and the pinchoff voltage is $V_P = -3.5\,\text{V}$. Calculate i_D and $v_{DS}(\text{sat})$ for $v_{GS} = 0$, $V_P/4$, and $V_P/2$.

Solution: From Equation (5.30), we have

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 = (2)\left(1 - \frac{v_{GS}}{(-3.5)}\right)^2$$

Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$i_D = 2, 1.13, \text{ and } 0.5\,\text{mA}$$

From Equation (5.31), we have

$$v_{DS}(\text{sat}) = v_{GS} - V_P = v_{GS} - (-3.5)$$

Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$v_{DS}(\text{sat}) = 3.5, 2.63, \text{ and } 1.75\,\text{V}$$

Comment: The current capability of a JFET can be increased by increasing the value of I_{DSS}, which is a function of the transistor width.

As for the MOSFET, the i_D versus v_{DS} characteristic may have a nonzero slope beyond the saturation point. This nonzero slope can be described through the following equation:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \quad \textbf{(5.33)}$$

where λ^{-1} is analogous to the Early voltage in bipolar transistors.

The output resistance r_o is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \quad \textbf{(5.34)}$$

Using Equation (5.33), we find that

$$r_o = \left[\lambda I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2\right]^{-1} \quad \textbf{(5.35(a))}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} \quad \textbf{(5.35(b))}$$

The output resistance will be considered again when we discuss the small-signal equivalent circuit of the JFET in the next chapter.

Enhancement-mode GaAs MESFETs can be fabricated with current–voltage characteristics much like those of the enhancement-mode MOSFET. Therefore, for the ideal enhancement-mode MESFET biased in the saturation region, we can write

$$i_D = K_n(v_{GS} - V_{TN})^2 \quad \textbf{(5.36(a))}$$

For the ideal enhancement-mode MESFET biased in the nonsaturation region,

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \quad \textbf{(5.36(b))}$$

where K_n is the conduction parameter and V_{TN} is the threshold voltage, which in this case is equivalent to the pinchoff voltage. For an n-channel enhancement-mode MESFET, the threshold voltage is positive.

Test Your Understanding

5.26 The parameters of an n-channel JFET are $I_{DSS} = 12\,\text{mA}$, $V_P = -4.5\,\text{V}$, and $\lambda = 0$. Determine $V_{DS}(\text{sat})$ for $V_{GS} = -1.2\,\text{V}$, and calculate I_D for $V_{DS} > V_{DS}(\text{sat})$. (Ans. $V_{DS}(\text{sat}) = 3.3\,\text{V}$, $I_D = 6.45\,\text{mA}$)

5.27 For an n-channel JFET, the parameters are: $I_{DSS} = 2\,\text{mA}$, $V_P = -2.5\,\text{V}$, and $\lambda = 0$. What is the value of V_{GS} when $I_D = 1.2\,\text{mA}$ and the transistor is biased in the saturation region? (Ans. $V_{GS} = -0.564\,\text{V}$)

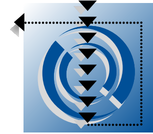
5.28 A p-channel JFET has a pinchoff voltage of $V_P = 3.8\,\text{V}$. The drain current in the saturation region is $I_D = 3\,\text{mA}$ when $V_{GS} = 0.8\,\text{V}$. Determine I_{DSS} and $V_{SD}(\text{sat})$. (Ans. $I_{DSS} = 4.81\,\text{mA}$, $V_{SD}(\text{sat}) = 3.0\,\text{V}$)

5.29 An n-channel GaAs MESFET has parameters $K_n = 25\,\mu\text{A/V}^2$ and $V_{TN} = 0.25\,\text{V}$. Determine I_D in the saturation region for: (a) $V_{GS} = 0.35\,\text{V}$, and (b) $V_{GS} = 0.50\,\text{V}$. (Ans. (a) $I_D = 0.25\,\mu\text{A}$, (b) $I_D = 1.56\,\mu\text{A}$)

5.4.3 Common JFET Configurations: DC Analysis

There are several common JFET circuit configurations. We will look at a few of these, using examples, and will illustrate the dc analysis and design of such circuits.

Design Example 5.17 **Objective:** Design the dc bias of a JFET circuit with an n-channel depletion-mode JFET.



For the circuit in Figure 5.56(a), the transistor parameters are: $I_{DSS} = 5\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_D = 2\,\text{mA}$ and $V_{DS} = 6\,\text{V}$.

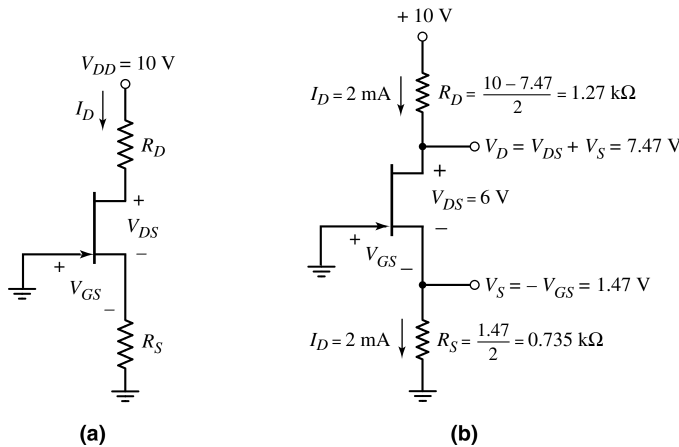


Figure 5.56 (a) An n-channel JFET circuit with a self-biasing source resistor and (b) circuit for Example 5.16

Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$2 = 5\left(1 - \frac{V_{GS}}{(-4)}\right)^2$$

Therefore,

$$V_{GS} = -1.47\,\text{V}$$

From Figure 5.56(b) we see that the current through the source resistor can be written as

$$I_D = \frac{-V_{GS}}{R_S}$$

Therefore,

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-1.47)}{2} = 0.735\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

Therefore,

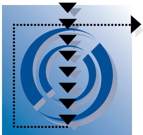
$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 6 - (2)(0.735)}{2} = 1.27\,\text{k}\Omega$$

We also see that

$$V_{DS} = 6\,\text{V} > V_{GS} - V_P = -1.47 - (-4) = 2.53\,\text{V}$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.

Comment: Since the source terminal must be positive with respect to the gate in order to bias the transistor on, the source resistor self-biases the JFET, even though the gate and the "bottom" of R_S are at ground potential.



Design Example 5.18 **Objective:** Design a JFET circuit with a voltage divider biasing circuit.

Consider the circuit shown in Figure 5.57(a) with transistor parameters $I_{DSS} = 12\,\text{mA}$, $V_P = -3.5\,\text{V}$, and $\lambda = 0$. Let $R_1 + R_2 = 100\,\text{k}\Omega$. Design the circuit such that the dc drain current is $I_D = 5\,\text{mA}$ and the dc drain-to-source voltage is $V_{DS} = 5\,\text{V}$.

Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore,

$$5 = 12\left(1 - \frac{V_{GS}}{(-3.5)}\right)^2$$

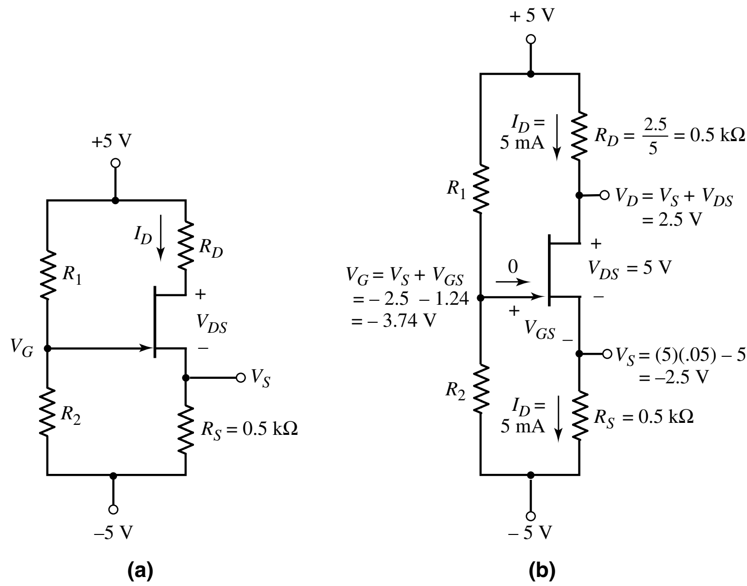


Figure 5.57 (a) An n-channel JFET circuit with voltage divider biasing and (b) the n-channel JFET circuit for Example 5.18

which yields

$$V_{GS} = -1.24\,\text{V}$$

From Figure 5.57(b), the voltage at the source terminal is

$$V_S = I_D R_S - 5 = (5)(0.5) - 5 = -2.5\,\text{V}$$

which means that the gate voltage is

$$V_G = V_{GS} + V_S = -1.24 - 2.5 = -3.74\,\text{V}$$

We can also write the gate voltage as

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5$$

or

$$-3.74 = \frac{R_2}{100}(10) - 5 \cdot$$

Therefore,

$$R_2 = 12.6\,\text{k}\Omega$$

and

$$R_1 = 87.4\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = 5 - I_D R_D - I_D R_S - (-5)$$

Therefore,

$$R_D = \frac{10 - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - (5)(0.5)}{5} = 0.5\,\text{k}\Omega$$

We also see that

$$V_{DS} = 5\,\text{V} > V_{GS} - V_P = -1.24 - (-3.5) = 2.26\,\text{V}$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.

Comment: The dc analysis of the JFET circuit is essentially the same as that of the MOSFET circuit, since the gate current is assumed to be zero.

Example 5.19 **Objective:** Calculate the quiescent current and voltage values in a p-channel JFET circuit.

The parameters of the transistor in the circuit shown in Figure 5.58 are: $I_{DSS} = 2.5\,\text{mA}$, $V_P = +2.5\,\text{V}$, and $\lambda = 0$. The transistor is biased with a constant- current source.

Solution: From Figure 5.58, we can write the dc drain current as

$$I_D = I_Q = 0.8\,\text{mA} = \frac{V_D - (-9)}{R_D}$$

which yields

$$V_D = (0.8)(4) - 9 = -5.8\,\text{V}$$

Now, assume the transistor is biased in the saturation region. We then have

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$0.8 = 2.5\left(1 - \frac{V_{GS}}{2.5}\right)^2$$

which yields

$$V_{GS} = 1.086\,\text{V}$$

Then

$$V_S = 1 - V_{GS} = 1 - 1.086 = -0.086\,\text{V}$$

and

$$V_{SD} = V_S - V_D = -0.086 - (-5.8) = 5.71\,\text{V}$$

Again, we see that

$$V_{SD} = 5.71\,\text{V} > V_P - V_{GS} = 2.5 - 1.086 = 1.41\,\text{V}$$

which verifies that the transistor is biased in the saturation region, as assumed.

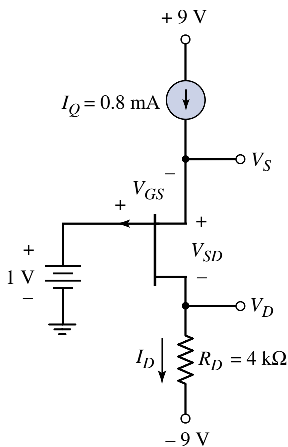
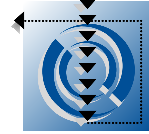


Figure 5.58 A p-channel JFET circuit biased with a constant-current source

Comment: In the same way as bipolar or MOS transistors, junction field-effect transistors can be biased using constant-current sources.

Design Example 5.20 **Objective:** Design a circuit with an enhancement-mode MESFET.



Consider the circuit shown in Figure 5.59(a). The transistor parameters are: $V_{TN} = 0.24\,\text{V}$, $K_n = 1.1\,\text{mA/V}^2$, and $\lambda = 0$. Let $R_1 + R_2 = 50\,\text{k}\Omega$. Design the circuit such that $V_{GS} = 0.50\,\text{V}$ and $V_{DS} = 2.5\,\text{V}$.

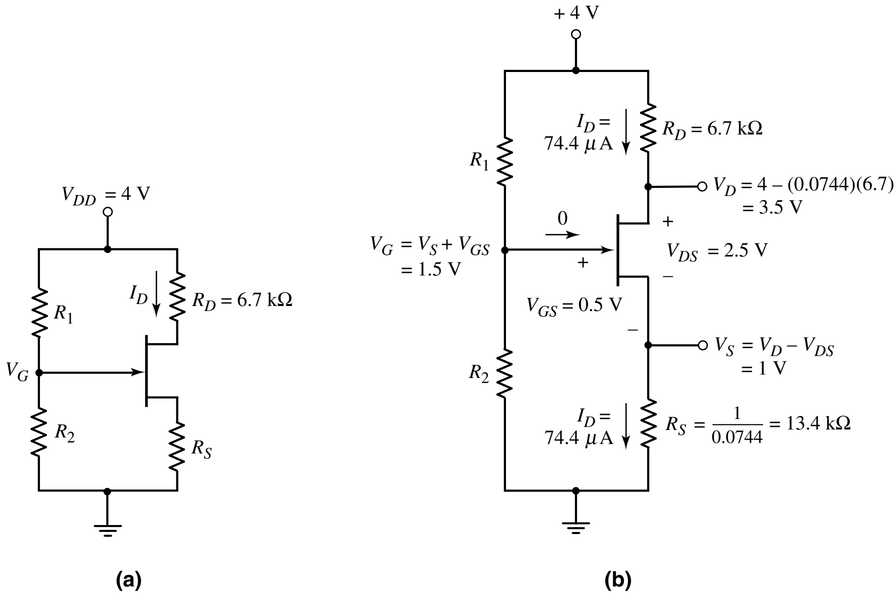


Figure 5.59 (a) An n-channel enhancement-mode MESFET circuit and (b) the n-channel MESFET circuit for Example 5.20

Solution: From Equation (5.36(a)) the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (1.1)(0.5 - 0.24)^2 = 74.4\,\mu\text{A}$$

From Figure 5.59(b), the voltage at the drain is

$$V_D = V_{DD} - I_D R_D = 4 - (0.0744)(6.7) = 3.5\,\text{V}$$

Therefore, the voltage at the source is

$$V_S = V_D - V_{DS} = 3.5 - 2.5 = 1\,\text{V}$$

The source resistance is then

$$R_S = \frac{V_S}{I_D} = \frac{1}{0.0744} = 13.4\,\text{k}\Omega$$

The voltage at the gate is

$$V_G = V_{GS} + V_S = 0.5 + 1 = 1.5\,\text{V}$$

Since the gate current is zero, the gate voltage is also given by a voltage divider equation, as follows:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

or

$$1.5 = \left(\frac{R_2}{50}\right)(4)$$

which yields

$$R_2 = 18.75\,\text{k}\Omega$$

and

$$R_1 = 31.25\,\text{k}\Omega$$

Again, we see that

$$V_{DS} = 2.5\,\text{V} > V_{GS} - V_{TN} = 0.5 - 0.24 = 0.26\,\text{V}$$

which confirms that the transistor is biased in the saturation region, as initially assumed.

Comment: The dc analysis and design of an enhancement-mode MESFET circuit is similar to that of MOSFET circuits, except that the gate-to-source voltage of the MESFET must be held to no more than a few tenths of a volt.

Test Your Understanding

5.30 For the circuit in Figure 5.60, the transistor parameters are: $V_P = -3.5\,\text{V}$, $I_{DSS} = 18\,\text{mA}$, and $\lambda = 0$. Calculate V_{GS} and V_{DS}. Is the transistor biased in the saturation or nonsaturation region? (Ans. $V_{GS} = -1.17\,\text{V}$, $V_{DS} = 7.43\,\text{V}$, saturation region)

5.31 The transistor in the circuit in Figure 5.61 has parameters $I_{DSS} = 6\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_{DQ} = 2.5\,\text{mA}$ and $V_{DS} = 6\,\text{V}$, and the total power dissipated in R_1 and R_2 is 2 mW. (Ans. $R_D = 1.35\,\text{k}\Omega$, $R_1 = 158\,\text{k}\Omega$, $R_2 = 42\,\text{k}\Omega$)

***5.32** For the p-channel transistor in the circuit in Figure 5.62, the parameters are: $I_{DSS} = 6\,\text{mA}$, $V_P = 4\,\text{V}$, and $\lambda = 0$. Calculate the quiescent values of I_D, V_{GS}, and V_{SD}. Is the transistor biased in the saturation or nonsaturation region? (Ans. $V_{GS} = 1.81\,\text{V}$, $I_D = 1.81\,\text{mA}$, $V_{SD} = 2.47\,\text{V}$, saturation region)

***D5.33** Consider the circuit shown in Figure 5.63 with transistor parameters $I_{DSS} = 8\,\text{mA}$, $V_P = 4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $R_{in} = 100\,\text{k}\Omega$, $I_{DQ} = 5\,\text{mA}$, and $V_{SDQ} = 12\,\text{V}$. (Ans. $R_D = 0.4\,\text{k}\Omega$, $R_1 = 387\,\text{k}\Omega$, $R_2 = 135\,\text{k}\Omega$)

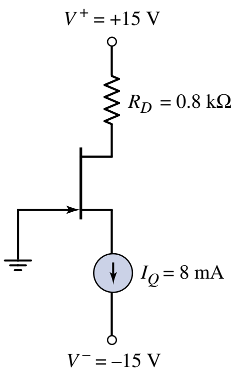


Figure 5.60 Circuit for Exercise 5.30

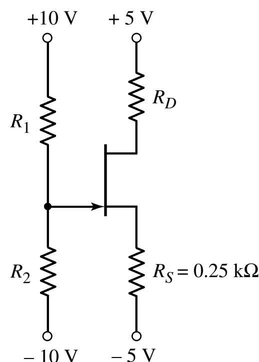


Figure 5.61 Circuit for Exercise 5.31

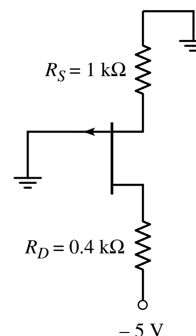


Figure 5.62 Circuit for Exercise 5.32

5.34 The n-channel enhancement-mode MESFET in the circuit shown in Figure 5.64 has parameters $K_n = 50\,\mu A/V^2$ and $V_{TN} = 0.15\,V$. Find the value of V_{GG} so that $I_{DQ} = 5\,\mu A$. What are the values of V_{GS} and V_{DS}? (Ans. $V_{GG} = 0.516\,V$, $V_{GS} = 0.466\,V$, $V_{DS} = 4.45\,V$)

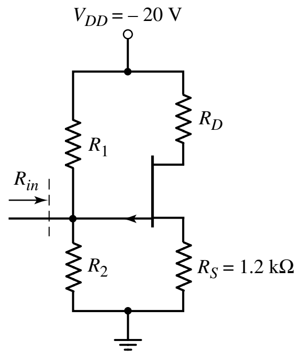


Figure 5.63 Circuit for Exercise 5.33

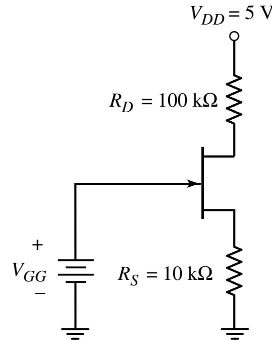


Figure 5.64 Circuit for Exercise 5.34

5.35 For the inverter circuit shown in Figure 5.65, the n-channel enhancement-mode MESFET parameters are $K_n = 100\,\mu A/V^2$ and $V_{TN} = 0.2\,V$. Determine the value of R_D required to produce $V_O = 0.10\,V$ when $V_I = 0.7\,V$. (Ans. $R_D = 267\,k\Omega$)

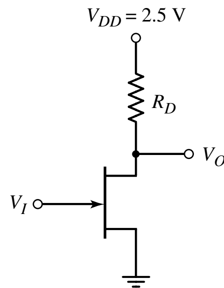


Figure 5.65 Circuit for Exercise 5.35

5.5 SUMMARY

- In this chapter, we have emphasized the structure and dc characteristics of the metal-oxide-semiconductor field-effect transistor (MOSFET). This device, because of its small size, has made possible the microprocessor and other high-density VLSI circuits, so this device is extremely important in integrated circuit technology.
- The current in the MOSFET is controlled by an electric field perpendicular to the surface of the semiconductor. This electric field is a function of the gate voltage. In the nonsaturation bias region of operation, the drain current is a function of the drain voltage, whereas in the saturation bias region of operation, the drain current is

essentially independent of the drain voltage. The drain current is directly proportional to the width-to-length ratio of the transistor, so this parameter becomes the primary design variable in MOSFET circuit design.

- The dc analysis and the design of dc biasing of MOSFET circuits were emphasized in this chapter. Several circuit configurations were analyzed and designed by using the ideal current-voltage relationships. The use of MOSFETs, both enhancement-mode and depletion-mode devices, in place of resistors was developed. This leads to the design of all-MOSFET circuits.
- Basic applications of the MOSFET were discussed. These include switching currents and voltages, performing digital logic functions, and amplifying time-varying signals. The amplifying characteristics will be considered in the next chapter and the important digital applications will be considered in Chapter 16.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Understand and describe the general operation of n-channel and p-channel enhancement-mode and depletion-mode MOSFETs. (Section 5.1)

✔ Understand the meaning of the various transistor parameters, including threshold voltage, width-to-length ratio, and drain-to-source saturation voltage. (Section 5.1)

✔ Apply the ideal current–voltage relations in the dc analysis and design of various MOSFET circuits using any of the four basic MOSFETs. (Section 5.2)

✔ Understand how MOSFETs can be used in place of resistor load devices to create all-MOSFET circuits. (Section 5.2)

✔ Qualitatively understand how MOSFETs can be used to switch currents and voltages, to perform digital logic functions, and to amplify time-varying signals. (Section 5.3)

✔ Understand the general operation and characteristics of junction FETs. (Section 5.4)

REVIEW QUESTIONS

1. Describe the basic operation of a MOSFET. Define enhancement mode and depletion mode.
2. Describe the general current–voltage characteristics for both enhancement-mode and depletion-mode MOSFETs.
3. Describe what is meant by threshold voltage, width-to-length ratio, and drain-to-source saturation voltage.
4. Define the saturation and nonsaturation bias regions.
5. Describe the channel length modulation effect and define the parameter λ. Describe the body effect and define the parameter γ,
6. Describe a simple common-source MOSFET circuit with an n-channel enhancement-mode device and discuss the relation between the drain-to-source voltage and gate-to-source voltage.
7. What are the steps in the dc analysis of a MOSFET circuit?
8. How do you prove that a MOSFET is biased in the saturation region?
9. In the dc analysis of some MOSFET circuits, quadratic equations in gate-to-source voltage are developed. How do you determine which of the two possible solutions is the correct one?
10. How can the Q-point be stabilized against variations in transistor parameters?

11. Describe the current–voltage relation of an n-channel enhancement-mode MOSFET with the gate connected to the drain.
12. Describe the current–voltage relation of an n-channel depletion-mode MOSFET with the gate connected to the source.
13. What is the principal difference between biasing techniques used in discrete transistor circuits and integrated circuits?
14. Describe how an n-channel enhancement-mode MOSFET can be used to switch a motor on and off.
15. Describe a MOSFET NOR logic circuit.
16. Describe how a MOSFET can be used to amplify a time-varying voltage.
17. Describe the basic operation of a junction FET.
18. What is the difference between a MESFET and a pn junction FET?

PROBLEMS

[Note: In all problems, assume the transistor parameter $\lambda = 0$, unless otherwise stated.]

Section 5.1 MOS Field-Effect Transistor

5.1 Consider an n-channel enhancement-mode MOSFET with parameters $V_{TN} = 1.5\,\text{V}$ and $K_n = 0.25\,\text{mA/V}^2$. Determine I_D for: (a) $V_{GS} = 5\,\text{V}$, $V_{DS} = 6\,\text{V}$; and (b) $V_{GS} = 5\,\text{V}$, $V_{DS} = 2.5\,\text{V}$.

5.2 The parameters of an n-channel enhancement-mode MOSFET are $V_{TN} = 0.8\,\text{V}$, $k'_n = 80\,\mu\text{A/V}^2$, and $W/L = 5$. (a) Assume the transistor is biased in the saturation region and $I_D = 0.5\,\text{mA}$. Determine $V_{DS}(\text{sat})$ and the required V_{GS}. (b) Repeat part (a) for $I_D = 1.5\,\text{mA}$.

5.3 For an n-channel depletion-mode MOSFET, the parameters are $V_{TN} = -2.5\,\text{V}$ and $K_n = 1.1\,\text{mA/V}^2$. (a) Determine I_D for $V_{GS} = 0$; and: (i) $V_{DS} = 0.5\,\text{V}$, (ii) $V_{DS} = 2.5\,\text{V}$, and (iii) $V_{DS} = 5\,\text{V}$. (b) Repeat part (a) for $V_{GS} = 2\,\text{V}$.

5.4 Consider an n-channel depletion-mode MOSFET with parameters $V_{TN} = -2\,\text{V}$ and $k'_n = 80\,\mu\text{A/V}^2$. The drain current is $I_D = 1.5\,\text{mA}$ at $V_{GS} = 0$ and $V_{DS} = 3\,\text{V}$. Determine the W/L ratio.

5.5 An n-channel enhancement-mode MOSFET has parameters $V_{TN} = 0.8\,\text{V}$, $W = 64\,\mu\text{m}$, $L = 4\,\mu\text{m}$, $t_{ox} = 450\,\text{Å}$, and $\mu_n = 650\,\text{cm}^2/\text{V–s}$. (a) Calculate the conduction parameter K_n. (b) Determine the drain current when $V_{GS} = V_{DS} = 3\,\text{V}$.

5.6 For a depletion NMOS device, the parameters are: $V_{TN} = -2\,\text{V}$, $\text{W} = 100\,\mu\text{m}$, $L = 5\,\mu\text{m}$, $t_{ox} = 600\,\text{Å}$, and $\mu_n = 500\,\text{cm}^2/\text{V–s}$. (a) Calculate the conduction parameter K_n. (b) Determine the drain current when: (i) $V_{GS} = 0$, $V_{DS} = 5\,\text{V}$, and (ii) $V_{GS} = 2\,\text{V}$, $V_{DS} = 1\,\text{V}$.

5.7 A particular NMOS device has parameters $V_{TN} = 1\,\text{V}$, $L = 2.5\,\mu\text{m}$, $t_{ox} = 400\,\text{Å}$, and $\mu_n = 600\,\text{cm}^2/\text{V–s}$. A drain current of $I_D = 1.2\,\text{mA}$ is requried when the device is biased in the saturation region at $V_{GS} = 5\,\text{V}$. Determine the necessary channel width of the device.

5.8 For a p-channel enhancement-mode MOSFET, $k'_p = 40\,\mu\text{A/V}^2$. The device has drain currents of $I_D = 0.225\,\text{mA}$ at $V_{SG} = V_{SD} = 3\,\text{V}$ and $I_D = 1.40\,\text{mA}$ at $V_{SG} = V_{SD} = 4\,\text{V}$. Determine the W/L ratio and the value of V_{TP}.

5.9 For a p-channel enhancement-mode MOSFET, the parameters are $K_P = 2\,\text{mA/V}^2$ and $V_{TP} = -0.5\,\text{V}$. The gate is at ground potential, and the source and substrate

terminals are at +5 V. Determine I_D when the drain terminal voltage is: (a) $V_D = 0\,\text{V}$, (b) $V_D = 2\,\text{V}$, (c) $V_D = 4\,\text{V}$, and (d) $V_D = 5\,\text{V}$.

5.10 A p-channel depletion-mode MOSFET has parameters $V_{TP} = +2\,\text{V}$, $k'_p = 40\,\mu\text{A/V}^2$, and $W/L = 6$. Determine $V_{SD}(\text{sat})$ for: (a) $V_{SG} = -1\,\text{V}$, (b) $V_{SG} = 0$, and (c) $V_{SG} = +1\,\text{V}$. If the transistor is biased in the saturation region, calculate the drain current for each value of V_{SG}.

5.11 Consider a p-channel depletion-mode MOSFET with parameters $K_P = 0.5\,\text{mA/V}^2$ and $V_{TP} = +2\,\text{V}$. If $V_{SG} = 0$, determine I_D for: (a) $V_{SD} = 1\,\text{V}$, (b) $V_{SD} = 2\,\text{V}$, and (c) $V_{SD} = 3\,\text{V}$.

D5.12 Enhancement-mode NMOS and PMOS devices both have parameters $L = 4\,\mu\text{m}$ and $t_{ox} = 500\,\text{Å}$. For the NMOS transistor, $V_{TN} = +0.6\,\text{V}$, $\mu_n = 675\,\text{cm}^2/\text{V–s}$, and the channel width is W_n; for the PMOS transistor, $V_{TP} = -0.6\,\text{V}$, $\mu_p = 375\,\text{cm}^2/\text{V–s}$, and the channel width is W_p. Design the widths of the two transistors such that they are electrically equivalent and the drain current in the PMOS transistor is $I_D = 0.8\,\text{mA}$ when it is biased in the saturation region at $V_{SG} = 5\,\text{V}$. What are the values of K_n, K_p, W_n, and W_p?

5.13 For an NMOS enhancement-mode transistor, the parameters are: $V_{TN} = 1.2\,\text{V}$, $K_n = 0.20\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Calculate the output resistance r_o for $V_{GS} = 2.0\,\text{V}$ and for $V_{GS} = 4.0\,\text{V}$. What is the value of V_A?

5.14 The parameters of an n-channel enhancement-mode MOSFET are $V_{TN} = 0.8\,\text{V}$, $k'_n = 80\,\mu\text{A/V}^2$, and $W/L = 4$. What is the maximum value of λ and the minimum value of V_A such that for $V_{GS} = 3\,\text{V}$, $r_o \geq 200\,\text{k}\Omega$?

5.15 An enhancement-mode NMOS transistor has parameters $V_{TNO} = 0.8\,\text{V}$, $\gamma = 0.8\,\text{V}^{1/2}$, and $\phi_f = 0.35\,\text{V}$. At what value of V_{SB} will the threshold voltage change by 2 V due to the body effect?

5.16 Consider an NMOS device with parameters $V_{TNO} = 1\,\text{V}$ and $\phi_f = 0.37\,\text{V}$. Determine the maximum value of γ such that the shift in threshold voltage between $V_{SB} = 0$ and $V_{SB} = 10\,\text{V}$ is no more than 1.2 V.

5.17 The silicon dioxide gate insulator of an MOS transistor has a thickness of $t_{ox} = 275\,\text{Å}$. (a) Calculate the ideal oxide breakdown voltage. (b) If a safety factor of three is required, determine the maximum safe gate voltage that may be applied.

5.18 In a power MOS transistor, the maximum applied gate voltage is 24 V. If a safety factor of three is specified, determine the minimum thickness necessary for the silicon dioxide gate insulator.

Section 5.2 Transistor DC Analysis

5.19 In the circuit in Figure P5.19, the transistor parameters are $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$. Calculate V_{GS}, I_D, and V_{DS}.

5.20 For the transistor in the circuit in Figure P5.20, the parameters are $V_{TN} = 2\,\text{V}$, $k'_n = 60\,\mu\text{A/V}^2$, and $W/L = 60$. Determine V_{GS}, I_D, and V_{DS}.

5.21 Consider the circuit in Figure P5.21. The transistor parameters are $V_{TP} = -2\,\text{V}$ and $K_p = 1\,\text{mA/V}^2$. Determine I_D, V_{SG}, and V_{SD}.

5.22 For the circuit in Figure P5.22, the transistor parameters are $V_{TP} = -0.8\,\text{V}$ and $K_p = 200\,\mu\text{A/V}^2$. Determine V_S and V_{SD}.

***D5.23** Design a MOSFET circuit in the configuration shown in Figure P5.19. The transistor parameters are $V_{TN} = 1.2\,\text{V}$, $k'_n = 60\,\mu\text{A/V}^2$, and $\lambda = 0$. The circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_D = 5\,\text{k}\Omega$. Design the circuit so that $V_{DSQ} \cong 5\,\text{V}$, the voltage across

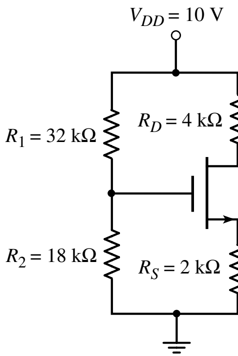


Figure P5.19

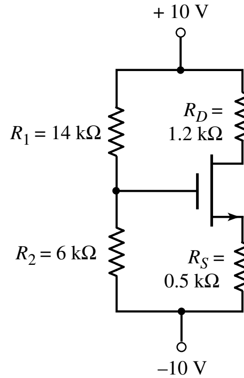


Figure P5.20

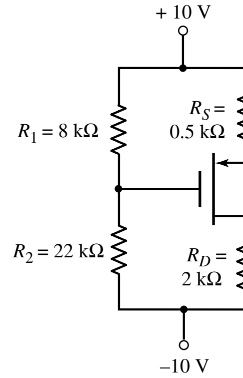


Figure P5.21

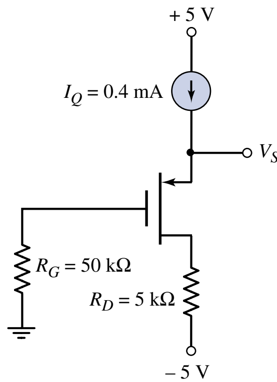


Figure P5.22

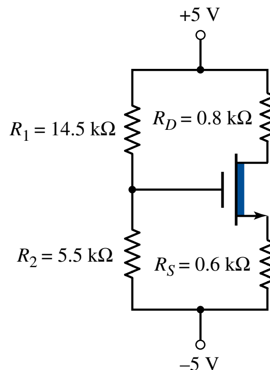


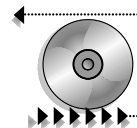
Figure P5.24

R_S is approximately equal to V_{GS}, and the current through the bias resistors is approximately 5 percent of the drain current.

5.24 The parameters of the transistor in the circuit in Figure P5.24 are $V_{TN} = -1\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$. Determine V_{GS}, I_D, and V_{DS}.

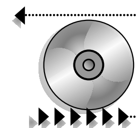
***D5.25** Design a MOSFET circuit with the configuration shown in Figure P5.21. The transistor parameters are $V_{TP} = -2\,\text{V}$, $k'_p = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The circuit bias is $\pm 10\,\text{V}$, the drain current is to be 0.8 mA, the drain-to-source voltage is to be approximately 10 V, and the voltage across R_S is to be approximately equal to V_{GS}. In addition, the current through the bias resistors is to be no more than 10 percent of the drain current.

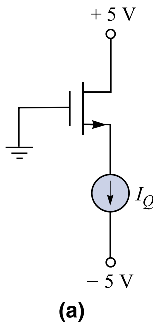
5.26 The parameters of the transistors in Figures P5.26(a) and (b) are $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 1.2\,\text{V}$, and $\lambda = 0$. Determine v_{GS} and v_{DS} for each transistor when (i) $I_Q = 50\,\mu\text{A}$ and (ii) $I_Q = 1\,\text{mA}$.



5.27 For the circuit in Figure P5.27, the transistor parameters are $V_{TN} = 0.6\,\text{V}$ and $K_n = 200\,\mu\text{A/V}^2$. Determine V_S and V_D.

D5.28 Design the circuit in Figure P5.28, such that $I_D = 0.8\,\text{mA}$ and $V_D = 1\,\text{V}$. The transistor parameters are $K_n = 400\,\mu\text{A/V}^2$ and $V_{TN} = 1.7\,\text{V}$.





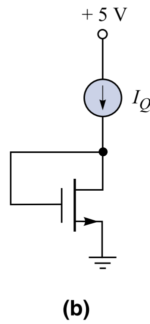


Figure P5.26

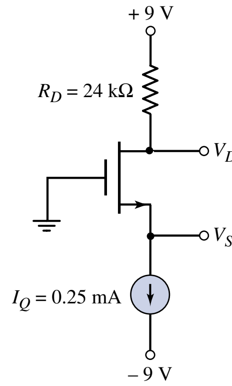


Figure P5.27

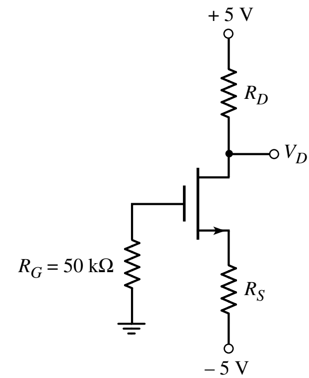


Figure P5.28

D5.29 The PMOS transistor in Figure P5.29 has parameters $V_{TP} = -1.5\,\text{V}$, $k_p' = 25\,\mu\text{A/V}^2$, $L = 4\,\mu\text{m}$, and $\lambda = 0$. Determine the values of W and R such that $I_D = 0.1\,\text{mA}$ and $V_{SD} = 2.5\,\text{V}$.

D5.30 Design the circuit in Figure P5.30 so that $V_{SD} = 2.5\,\text{V}$. The current in the bias resistors should be no more than 10 percent of the drain current. The transistor parameters are $V_{TP} = +1.5\,\text{V}$ and $K_p = 0.5\,\text{mA/V}^2$.

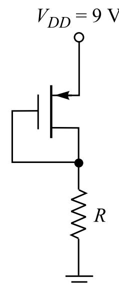


Figure P5.29

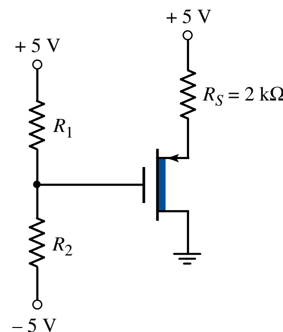


Figure P5.30

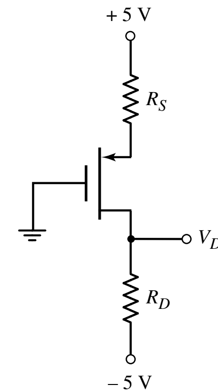
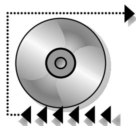


Figure P5.31

D5.31 Design the circuit in Figure P5.31 such that $I_D = 0.5\,\text{mA}$ and $V_D = -3\,\text{V}$. The transistor parameters are $k_p' = 30\,\mu\text{A/V}^2$, $W/L = 20$, and $V_{TP} = -1.2\,\text{V}$.

D5.32 The parameters of the transistor in the circuit in Figure P5.32 are $V_{TP} = -1.75\,\text{V}$ and $K_p = 3\,\text{mA/V}^2$. Design the circuit such that $I_D = 5\,\text{mA}$, $V_{SD} = 6\,\text{V}$, and $R_{\text{in}} = 80\,\text{k}\Omega$.



***5.33** For each transistor in the circuit in Figure P5.33, $k_n' = 60\,\mu\text{A/V}^2$. Also for M_1, $W/L = 4$ and $V_{TN} = +0.8\,\text{V}$, and for M_2, $W/L = 1$ and $V_{TN} = -1.8\,\text{V}$. Determine the region of operation of each transistor and the output voltage v_O for: (a) $v_I = 1\,\text{V}$, (b) $v_I = 3\,\text{V}$, and (c) $v_I = 5\,\text{V}$.

***D5.34** Consider the circuit in Figure P5.33. The transistor parameters are for M_1, $V_{TN} = +0.8\,\text{V}$ and $k_n' = 40\,\mu\text{A/V}^2$, and for M_2, $V_{TN} = -2\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $W/L = 1$. Determine the W/L ratio for M_1 such that $v_O = 0.15\,\text{V}$ when $v_I = 5\,\text{V}$.

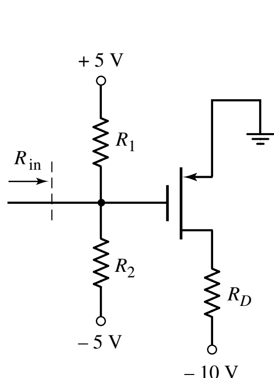


Figure P5.32

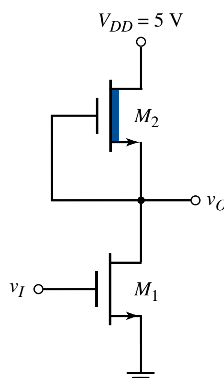


Figure P5.33

***5.35** The transistors in the circuit in Figure P5.35 both have parameters $V_{TN} = 0.8\,\text{V}$ and $k_n' = 30\,\mu\text{A/V}^2$. (a) If the width-to-length ratios of M_1 and M_2 are $(W/L)_1 = (W/L)_2 = 40$, determine V_{GS1}, V_{GS2}, V_O, and I_D. (b) Repeat part (a) if the width-to-length ratios are changed to $(W/L)_1 = 40$ and $(W/L)_2 = 15$.

D5.36 Consider the circuit in Figure P5.36. The transistor parameters are $V_{TN} = 1\,\text{V}$ and $k_n' = 36\,\mu\text{A/V}^2$. Design the width-to-length ratio required in each transistor such that $I_D = 0.5\,\text{mA}$, $V_1 = 2\,\text{V}$, and $V_2 = 5\,\text{V}$.

D5.37 The transistors in the circuit in Figure 5.35 in the text have parameters $V_{TN} = 0.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The width-to-length ratio of M_L is $(W/L)_L = 1$. Design the width-to-length ratio of the driver transistor such that $V_O = 0.10\,\text{V}$ when $V_I = 5\,\text{V}$.

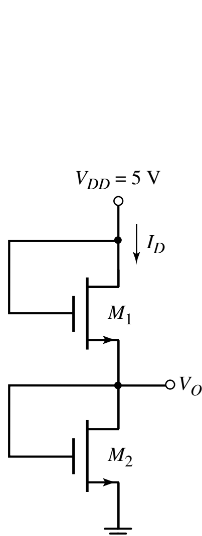


Figure P5.35

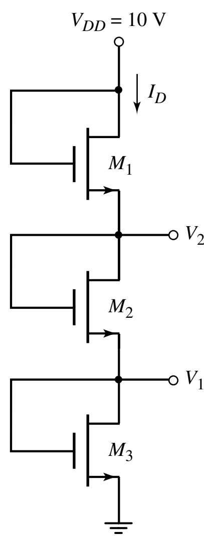


Figure P5.36

D5.38 For the circuit in Figure 5.39 in the text, the transistor parameters are: $V_{TND} = 0.8\,\text{V}$, $V_{TNL} = -1.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. Let $V_{DD} = 5\,\text{V}$. The width-to-length ratio of M_L is $(W/L)_L = 1$. Design the width-to-length ratio of the driver transistor such that $V_O = 0.05\,\text{V}$ when $V_I = 5\,\text{V}$.

5.39 All transistors in the circuit in Figure 5.43 in the text have parameters $V_{TN} = 1\,\text{V}$ and $\lambda = 0$. Assume the conduction parameters are $K_{n1} = 80\,\mu\text{A/V}^2$, $K_{n2} = 100\,\mu\text{A/V}^2$, $K_{n3} = 200\,\mu\text{A/V}^2$, and $K_{n4} = 400\,\mu\text{A/V}^2$. Determine I_{REF}, I_Q, and each gate-to-source voltage.

Section 5.3 MOSFET Switch and Amplifier

5.40 Consider the circuit in Figure P5.40. The transistor parameters are $V_{TN} = 0.8\,\text{V}$ and $k_n' = 30\,\mu\text{A/V}^2$. The resistor is $R_D = 10\,\text{k}\Omega$. Determine the transistor width-to-length ratio (W/L) such that $V_O = 0.1\,\text{V}$ when $V_I = 4.2\,\text{V}$.

D5.41 The transistor in the circuit in Figure P5.41 is used to turn the LED on and off. The transistor parameters are $V_{TN} = 0.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The diode cut-in voltage is $V_\gamma = 1.6\,\text{V}$. Design R_D and the transistor W/L ratio such that $I_D = 12\,\text{mA}$ for $V_I = 5\,\text{V}$ and $V_{DS} = 0.2\,\text{V}$.

D5.42 The circuit in Figure P5.42 is another configuration used to switch an LED on and off. The transistor parameters are $V_{TP} = -0.8\,\text{V}$, $k_p' = 20\,\mu\text{A/V}^2$, and $\lambda = 0$. The diode cut-in voltage is $V_\gamma = 1.6\,\text{V}$. Design R_D and the transistor W/L ratio such that $I_D = 15\,\text{mA}$ for $V_I = 0\,\text{V}$ and $V_{SD} = 0.15\,\text{V}$.

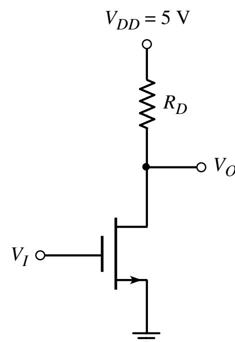


Figure P5.40

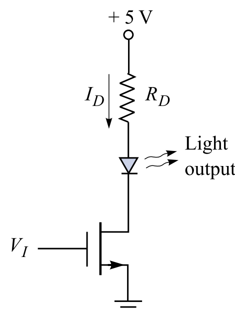


Figure P5.41

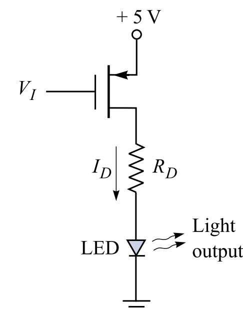


Figure P5.42

Section 5.4 Junction Field-Effect Transistor

5.43 The gate and source of an n-channel depletion-mode JFET are connected together. What value of V_{DS} will ensure that this two-terminal device is biased in the saturation region. What is the drain current for this bias condition?

5.44 For an n-channel JFET, the parameters are $I_{DSS} = 6\,\text{mA}$ and $V_P = -3\,\text{V}$. Calculate $V_{DS}(\text{sat})$. If $V_{DS} > V_{DS}(\text{sat})$, determine I_D for: (a) $V_{GS} = 0$, (b) $V_{GS} = -1\,\text{V}$, (c) $V_{GS} = -2\,\text{V}$, and (d) $V_{GS} = -3\,\text{V}$.

5.45 A p-channel JFET biased in the saturation region with $V_{SD} = 5\,\text{V}$ has a drain current of $I_D = 2.8\,\text{mA}$ at $V_{GS} = 1\,\text{V}$ and $I_D = 0.30\,\text{mA}$ at $V_{GS} = 3\,\text{V}$. Determine I_{DSS} and V_P.

5.46 Consider the p-channel JFET in Figure P5.46. Determine the range of V_{DD} that will bias the transistor in the saturation region. If $I_{DSS} = 6\,\text{mA}$ and $V_P = 2.5\,\text{V}$, find V_S.

5.47 Consider a GaAs MESFET. When the device is biased in the saturation region, we find that $I_D = 18.5\,\mu\text{A}$ at $V_{GS} = 0.35\,\text{V}$ and $I_D = 86.2\,\mu\text{A}$ at $V_{GS} = 0.50\,\text{V}$. Determine the conduction parameter k and the threshold voltage V_{TN}.

5.48 The threshold voltage of a GaAs MESFET is $V_{TN} = 0.24\,\text{V}$. The maximum allowable gate-to-source voltage is $V_{GS} = 0.75\,\text{V}$. When the transistor is biased in the saturation region, the maximum drain current is $I_D = 250\,\mu\text{A}$. What is the value of the conduction parameter k?

***5.49** For the transistor in the circuit in Figure P5.49, the parameters are: $I_{DSS} = 10\,\text{mA}$ and $V_P = -5\,\text{V}$. Determine I_{DQ}, V_{GSQ}, and V_{DSQ}.

D5.50 Consider the source follower with the n-channel JFET in Figure P5.50. The input resistance is to be $R_{\text{in}} = 500\,\text{k}\Omega$. We wish to have $I_{DQ} = 5\,\text{mA}$, $V_{DSQ} = 8\,\text{V}$, and $V_{GSQ} = -1\,\text{V}$. Determine R_S, R_1, and R_2, and the required transistor values of I_{DSS} and V_P.

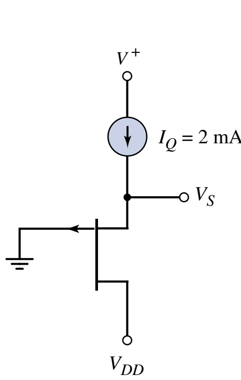


Figure P5.46

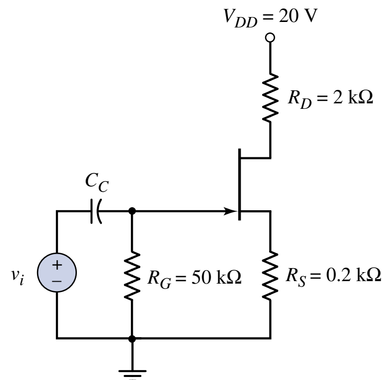


Figure P5.49

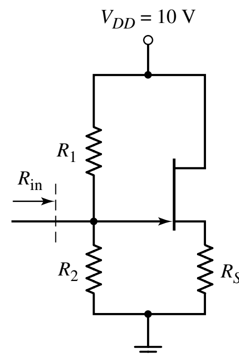


Figure P5.50

D5.51 The transistor in the circuit in Figure P5.51 has parameters $I_{DSS} = 8\,\text{mA}$ and $V_P = 4\,\text{V}$. Design the circuit such that $I_D = 5\,\text{mA}$. Assume $R_{\text{in}} = 100\,\text{k}\Omega$. Determine V_{GS} and V_{SD}.

D5.52 For the circuit in Figure P5.52, the transistor parameters are $I_{DSS} = 7\,\text{mA}$ and $V_P = 3\,\text{V}$. Let $R_1 + R_2 = 100\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 5.0\,\text{mA}$ and $V_{SDQ} = 6\,\text{V}$.

5.53 The transistor in the circuit in Figure P5.53 has parameters $I_{DSS} = 8\,\text{mA}$ and $V_P = -4\,\text{V}$. Determine V_G, I_{DQ}, V_{GSQ}, and V_{DSQ}.

5.54 Consider the circuit in Figure P5.54. The quiescent value of V_{DS} is found to be $V_{DSQ} = 5\,\text{V}$. If $I_{DSS} = 10\,\text{mA}$, determine I_{DQ}, V_{GSQ}, and V_P.

D5.55 For the circuit in Figure P5.55, the transistor parameters are $I_{DSS} = 4\,\text{mA}$ and $V_P = -3\,\text{V}$. Design R_D such that $V_{DS} = |V_P|$. What is the value of I_D?

D5.56 Consider the source-follower circuit in Figure P5.56. The transistor parameters are $I_{DSS} = 2\,\text{mA}$ and $V_P = 2\,\text{V}$. Design the circuit such that $I_{DQ} = 1\,\text{mA}$, $V_{SDQ} = 10\,\text{V}$, and the current through R_1 and R_2 is 0.1 mA.

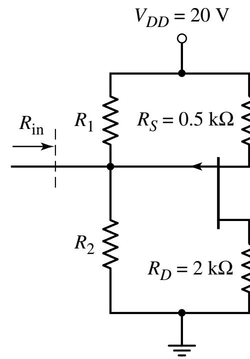


Figure P5.51

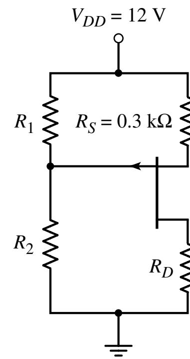


Figure P5.52

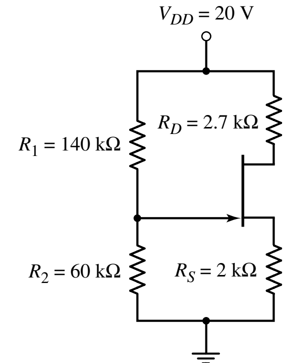


Figure P5.53

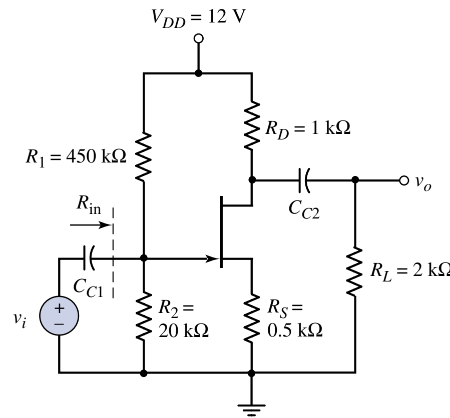


Figure P5.54

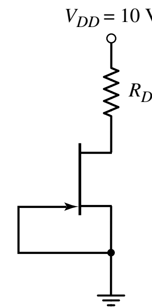


Figure P5.55

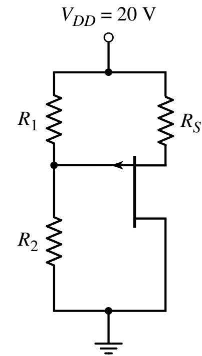


Figure P5.56

D5.57 The GaAs MESFET in the circuit in Figure P5.57 has parameters $k = 250\ \mu\text{A/V}^2$ and $V_{TN} = 0.20$ V. Let $R_1 + R_2 = 150$ kΩ. Design the circuit such that $I_D = 40\ \mu\text{A}$ and $V_{DS} = 2$ V.

5.58 For the circuit in Figure P5.58, the GaAs MESFET threshold voltage is $V_{TN} = 0.15$ V. Let $R_D = 50$ kΩ. Determine the value of the conduction parameter required so that $V_O = 0.70$ V when $V_I = 0.75$ V.

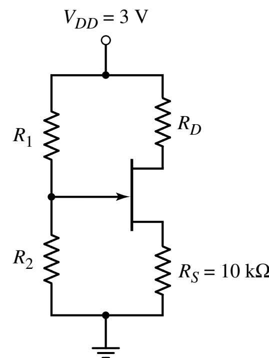


Figure P5.57

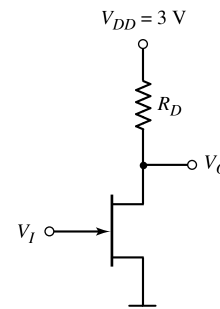


Figure P5.58

COMPUTER SIMULATION PROBLEMS

5.59 Generate the i_D versus v_{DS} characteristics for an n-channel enhancement-mode silicon MOSFET at $T = 300\,^\circ K$. Limit the characteristics to $v_{DS}(\max) = 10\,V$ and $v_{GS}(\max) = 10\,V$. Plot curves for: (a) $W/L = 4$, $\lambda = 0$; (b) $W/L = 40$, $\lambda = 0$; and (c) $W/L = 4$, $\lambda = 0.02\,V^{-1}$.

5.60 Consider the NMOS circuit with enhancement load shown in Figure 5.35. Assume a width-to-length ratio of $W/L = 1$ for M_L. From a computer analysis, plot the dc voltage transfer characteristics V_O versus V_I for M_D width-to-length ratios of: (a) $W/L = 2$, (b) $W/L = 9$, (c) $W/L = 16$, and (d) $W/L = 100$. Consider the case when the body effect is neglected, and then when the body effect is included.

5.61 Consider the NMOS circuit with depletion load shown in Figure 5.39. Use a computer analysis to plot the dc voltage transfer characteristics V_O versus V_I for the same parameters listed in Problem 5.60. Consider the case when the body effect is neglected, and then when the body effect is included.

5.62 (a) Correlate the results of Example 5.13 with a computer analysis. (b) Repeat the analysis if the width-to-length ratio of M_3 is doubled.

5.63 Correlate the JFET design in Example 5.18 with a computer analysis.

DESIGN PROBLEMS

[Note: All design should be correlated with a computer simulation.]

***D5.64** Consider a discrete common-source circuit with the configuration shown in Figure 5.29. The circuit and transistor parameters are: $V_{DD} = 10\,V$, $R_S = 0.5\,k\Omega$, $R_D = 4\,k\Omega$, and $V_{TN} = 2\,V$. Design the circuit such that the nominal Q-point is midway between the transition point and cutoff, and determine the conduction parameter. The dc currents in R_1 and R_2 should be approximately a factor of ten smaller than the quiescent drain current.

***D5.65** For the circuit shown in Figure 5.43, the threshold voltage of each transistor is $V_{TN} = 1\,V$, and the parameter value $k_n' = 40\,\mu A/V^2$ is the same for all devices. If $R_D = 4\,k\Omega$, design the cicuit such that the quiescent drain-to-source voltage of M_1 is $4\,V$ and $I_Q = \left(\frac{1}{2}\right) I_{REF}$.

***D5.66** The NMOS circuit with depletion load shown in Figure 5.39 is biased at $V_{DD} = 5\,V$. The threshold voltage of M_D is $V_{TND} = 0.8\,V$ and that of M_L is $V_{TNL} = -2\,V$. For each transistor, $k_n' = 40\,\mu A/V^2$. Design the transistors such that $V_O = 0.1\,V$ when $V_I = 5\,V$ and the maximum power dissipated in the circuit is 1.0 mW.

***D5.67** The threshold voltage of the load transistor M_L in Figure 5.35 is $V_{TNL} = 0.8\,V$. All other parameters are the same as given in Problem 5.66. Design the transistors to meet the same specifications given in Problem 5.66.

***D5.68** Consider the JFET common-source circuit shown in Figure 5.57(a). The transistor pinchoff voltage is $V_P = -4\,V$ and the saturation current is in the range $1 \le I_{DSS} \le 2\,mA$. Design the circuit such that the nominal Q-point is in the center of the load line and the Q-point parameters do not deviate from the nominal value by more than 10 percent. The value of R_S may be changed, the current in R_1 and R_2 should be approximately a factor of ten less than the quiescent drain current, and the standard tolerance resistance value of 5 percent should be used.