UNIT III - PERIPHERAL INTERFACING

INTRODUCTION

Microprocessor based system design involves interfacing of the processor with one or more peripheral devices for the purpose of communication with various input and output devices connected to it. During the early days of the microprocessor revolution, these techniques required complex hardware consisting of Medium scale integration devices making the design highly complex and time consuming. So, the manufacturers (INTEL) have developed a large number of general and special purpose peripheral devices most of them being single chip circuits. They are also programmable devices. Hence these peripheral devices are found to be of tremendous use to a system designer.

Peripheral devices can broadly be classified into two categories.

(a) General purpose peripherals and

(b) Special purpose peripherals (Dedicated function peripherals)

General purpose peripheral devices that perform a task but may be used for interfacing a variety of I/O devices to microprocessor. The general purpose devices are given below:

- Simple I/O -- (Non-programmable)
  - Programmable peripheral Interface (PPI) – (8255)
  - Programmable Interrupt Controller – (8259)
  - Programmable DMA Controller – (8237/8257)
  - Programmable Communication Interface – (8251)
  - Programmable Interval Timer – (8253/8254)

Special function peripherals are devices that may be used for interfacing a microprocessor to a specific type of I/O device. These peripherals are more complex and therefore, relatively more expensive than general purpose peripherals. The special function peripherals (Dedicated function peripherals) are

- Programmable CRT Controller
- Programmable Floppy Disc Controller
- Programmable Hard Disc Controller
- Programmable Keyboard and display interface.

The functioning of these devices varies depending on the type of I/O device they are controlling.

8255 - PROGRAMMABLE PERIPHERAL INTERFACING(8255 - PPI):

- **8255** is a widely used, programmable, parallel I/O device.
- It can be programmed to transfer data under various conditions from simple I/O to interrupt I/O.

Introduction

INTEL introduced this programmable peripheral interface (PPI) chip 8255A for interfacing peripheral devices to the 8085 system. This versatile chip 8255A is used as a general purpose peripheral device for parallel data transfer between microprocessor and a peripheral device by interfacing the device to the system data bus. The PPI has three programmable I/O ports viz., Port A, Port B and Port C each of 8 bit width. Port C can be treated as two ports – Port C upper (PC_7-4) and Port lower (PC_3 – 0) and these two can be independently programmed as INPUT or OUTPUT ports also.

- **Salient Features**

i. It is a general purpose programmable I/O device which is compatible with all INTEL processors and also most other processors.

ii. It provides 24 I/O pins which may be individually programmed in two groups.

iii. This chip is also completely TTL compatible.

Iv .It is available in 40 pin DIP and 44 pin plastic leaded chip carrier (PLCC) packages.

v. It has three 8 bit ports. Port A, Port B and Port C. Port C is treated as two 4 bit ports also.

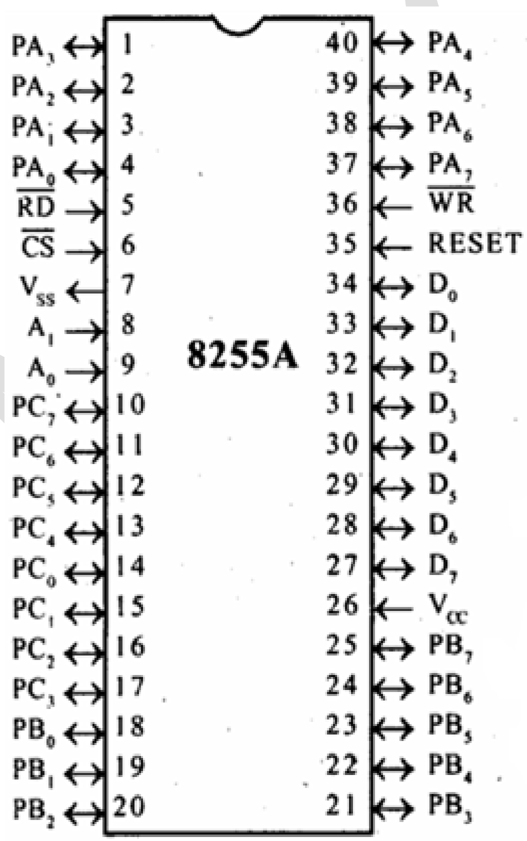
vi. This 8255 is mainly programmed in two modes (a) the I/O mode and (b) The bit set/reset mode (BSR) mode. The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2.

vii. An 8 bit control resister is used to configure the modes of 8255.

There is also another 8 bit port called control port, which decides the configuration of 8255 ports. This port is written by the microprocessor only.

PIN CONFIGURATION OF 8255:

- **D_0-D_7 (DataBus):** Bidirectional, tri-state, databus lines connectedto the system data bus.They are used to transfer data and control word from microprocessor to 8255 or receive data or status word from 8255 to 8085.
- **PA_0-PA_7(PortA):** These 8-bit bidirectional I/O pins are used to send or receive data from O/P or I/P device.
- **PB_0-PB_7(Port B):** These 8-bitbidirectionalI/Opins areused to send or receive datafrom O/P or I/P device.



Pin	Description
D_0 - D_7	Data lines
RESET	Reset input
$\overline{CS}$	Chip select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
A_0, A_1	Internal address
PA_7 - PA_0	Port-A pins
PB_7 - PB_0	Port-B pins
PC_7 - PC_0	Port-C pins
V_{CC}	+5V
V_{SS}	0V (GND)

Figure 1: Pin Diagram of 8255 **Table 1: Pin Description**

- **PC_0- PC_7(port C):** These 8-bit bidirectional I/O pins are divided into two groups PC_L (PC_0- PC_3)and PC_U (PC_4- PC_7). These groups can individually transfer data in or out when programmed I/O. When programmed in bidirectional or handshake modes these bits are used as handshake signals.
- **RD' (Read):** MPU or CPU reads data in the ports or the status word through data buffer.
- **WR' (Write):** MPU or CPU writes data in the ports or the control register through data Buffer.
- **CS' (Chip Select):** It is an active below inputwhichcan be used to enable 8255for data transfer operation betweenCPU (MPU) and 8255.
- **RESET:** It is an active high input used to reset 8255. When reset input is high, the control register is cleared and allthe ports are set to the input mode. Usually RESETOUT signal from 8085 is used to reset 8255.
- **A_0&A_1:** These input signals along with RD', WR' inputs control the selection of control / status word registers or one of three ports.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

Table 2: Control Word Register

BLOCK DIAGRAM OF 8255:

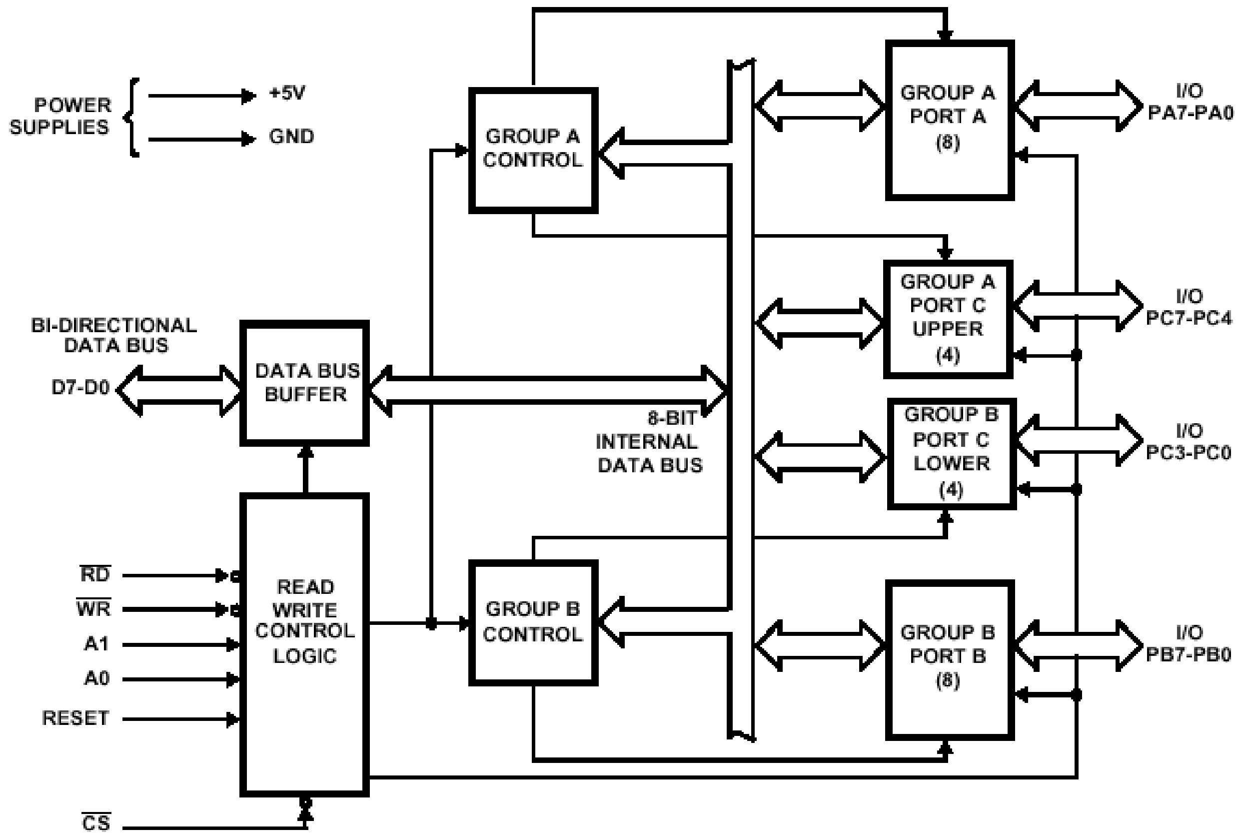


Figure 2: Block Diagram of 8255

- **Data Bus buffer :**

  Tri-state bidirectional buffer is usedto interface the internal data bus of8255 to the system data bus. Output data from the MPU to the ports or control register and the input datato the MPU from the ports or status register are all pushed through the buffer.

- **Control Logic**

  This block accepts control bus signalsas well as inputs from the address bus and issues commands to the individual groupcontrol blocks (Group A Control and GroupBControl)as shown in Fig.2.

- **Group AControl and Group B Control**

  GroupA control block controls PortA and PC7-PC4.Group B controls block controlsPort Band PC_3- PC_0.

- **PortA**

  This has 8-bit latched and buffered output and an 8-bit input latch. It can be programmedinthreemodes:

  Mode 0:SimpleI/Omode

  Mode 1: I/OwithHandshakingmode

  Mode 2: Bidirectionaldatatransfermode.

- **Port B**

  This has 8-bit I/O latch/buffer and an 8-bit data input buffer. It can be programmed in mode 0 or mode 1.

- **Port C**

  This has 8-bit unlatched input buffer and an 8-bit output latch/buffer. Port C can besplittedintotwo parts and each bit can be used as control signals for Port A and Port B inhandshake mode. It can be programmed for BSR (Bit Set / Reset mode) operation.

Modes of Operation:

1. BSRmode
2. I/O mode
   - Mode 0: SimpleI/Omode
   - Mode 1 : I/OwithHandshakingmode
   - Mode 2: Bidirectionaldatatransfermode

1. BSR (Bit Set/Reset) Mode:

Individual bits of Port C can be set or reset by sending out a single OUT instruction to the control register. When Port C is used for control/status operation, this feature can be used to set or reset individual bits. For BSR mode control word is given below.

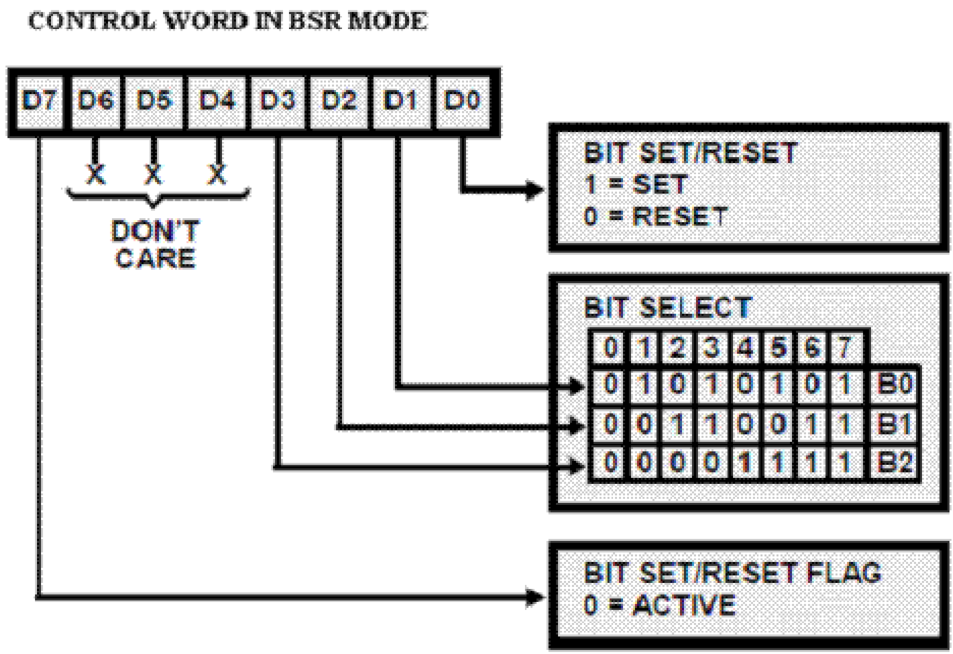


Figure 3:Control word for BSR mode

A BSR word is to be written for each bit that is to be set or reset. The BSR word can also be used for enabling or disabling the interrupt signals generated by Port c when 8255is programmed for mode 1or mode2 operation.

2. **I/O mode:**

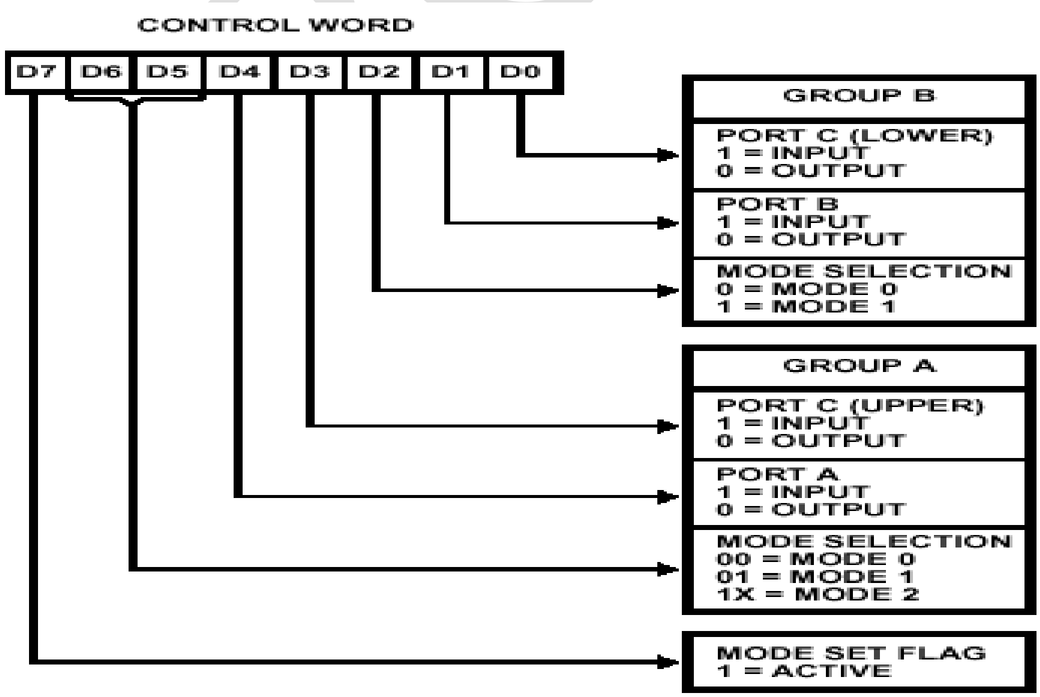


Figure 4: Control word format for I/O mode

i) **Mode 0 : Basic Input/output**

This mode provides simple input and output operations for each of the three ports. Data issimply written to or read from a specified port.

Basic functional definition

In mode 0:

- Therearetwo8-bitports (A and B) and two 4-bit ports [C (lower)] and [C (upper)].
- Any port can be an input port or an output port.
- Outputs are latched.
- Inputs are not latched.
- 16 different input/output configurations are possible in this mode.

ii) **Mode1: StrobedInput/Output**

It provides means for transferring I/O data to or from a specified port in conjunction withstrobes or hand-shaking signals. Port A and port B use the lines on port C for handshaking signals.

Basicfunctionaldefinition

In mode1:

- Thereare two groups (Group A and B). .
- Each group contains one 8-bit data port and one 4-bit control data port.
- The 8-bit data port can be either an input port or an output port. Both inputs and outputs are latched.
- The4-bit port is used for control as well as for status of the 8-bit data port.

iii) **Mode2 : Strobed BidirectionalBus**

This functional configuration provides a means for communicating with a peripheral device or Structure on a single 8-bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain a proper bus flow discipline.Interrupt generation and enable/disableFunctions are also available.

Basicfunctional definition

In mode 2 (used in GroupA only):

- There is one 8-bit bidirectional bus port (port A) and a 5-bit control port (port C)
- Both inputs and outputs are latched.

- The 5-bit control port (port C) is used for control as well as for status of the 8-bit bidirectionalbus port (portA).

PROGRAMMABLE INTERRUPT CONTROLLER (PIC) - 8259

Introduction

There is an absolute need of this Programmable Interrupt Controller for Interfacing I/O devices to the microprocessor. The 8085 processor has 5 interrupt lines namely, Trap, RST 7.5, RST 6.5, RST 5.5 and INTR. So, we can interface five I/O devices, which can perform the interrupt driven data transfer safely. But, suppose we wish to connect more than five I/O devices, to the microprocessor, then we may have to connect more than one I/O device to the interrupt lines. This will affect the interrupt driven data transfer and the microprocessor has to perform polling. i.e, it has to check each device, which is in need of interrupt service. This polling has the dis-advantage of long time and slow interrupt response. Hence to overcome all these problems, INTEL introduced the 28 pin DIP chip -8259. This device accepts interrupt requests from as many as 8 devices independently and as many as 64 I/O devices by cascading method.

Salient Features

INTEL 8259 is a single chip programmable interrupt controller which is compatible with 8085, 8086 and 8088 processors.

- It is a 28 pin DIP IC with N-Mos technology and requires a single +5 DC supply.
- It handles up to eight vectored priority interrupts for the CPU and cascadable for up to 64 vectored priority interrupts without the need of any additional circuitry.
- when two 8259s are cascaded through cascade lines the first 8259 will act as master and the second 8259 will act as a slave.

PIN CONFIGURATION OF 8529

The pin diagram of 8259 is shown below . The pin details are given below

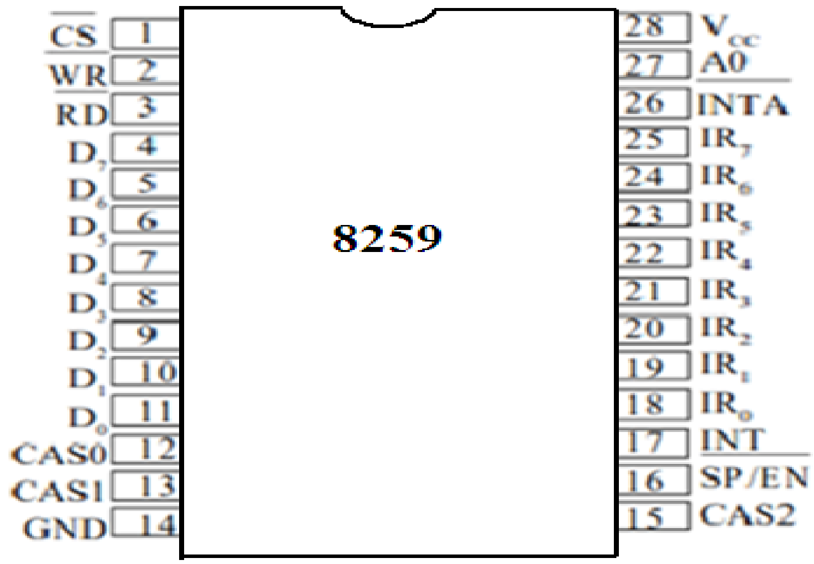


Figure 5:Pin Diagram of 8259

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

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BLOCK DIAGRAM OF 8259

The block diagram of programmable interrupt controller is shown in Fig. below. The block diagram consists of eight sub units. They are Control logic, Read/write logic, Data bus buffer. Three register (IRR, ISR and IMR), 5 priority resolver and cascade buffer. The functions of each unit are explained below.

Interrupt Request Register (IRR) & Interrupt Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic unit determines the priorities of the bits set in the IRR. The highest priority is selected and strobed in to the corresponding bit of the ISR during pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

Control Logic

This unit has two pins. INT (Interrupt) as an output pin and (interrupt acknowledge) as an input pin. The INT is connected to the interrupt pin of the microprocessor unit. Whenever an interrupt is noticed by the CPU, it generates signal

. **Cascade Buffer**

This function block stores the IDs of all 8259A are used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0 –2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive INTA pulses. (See section ‘‘Cascading the 8259A’’.

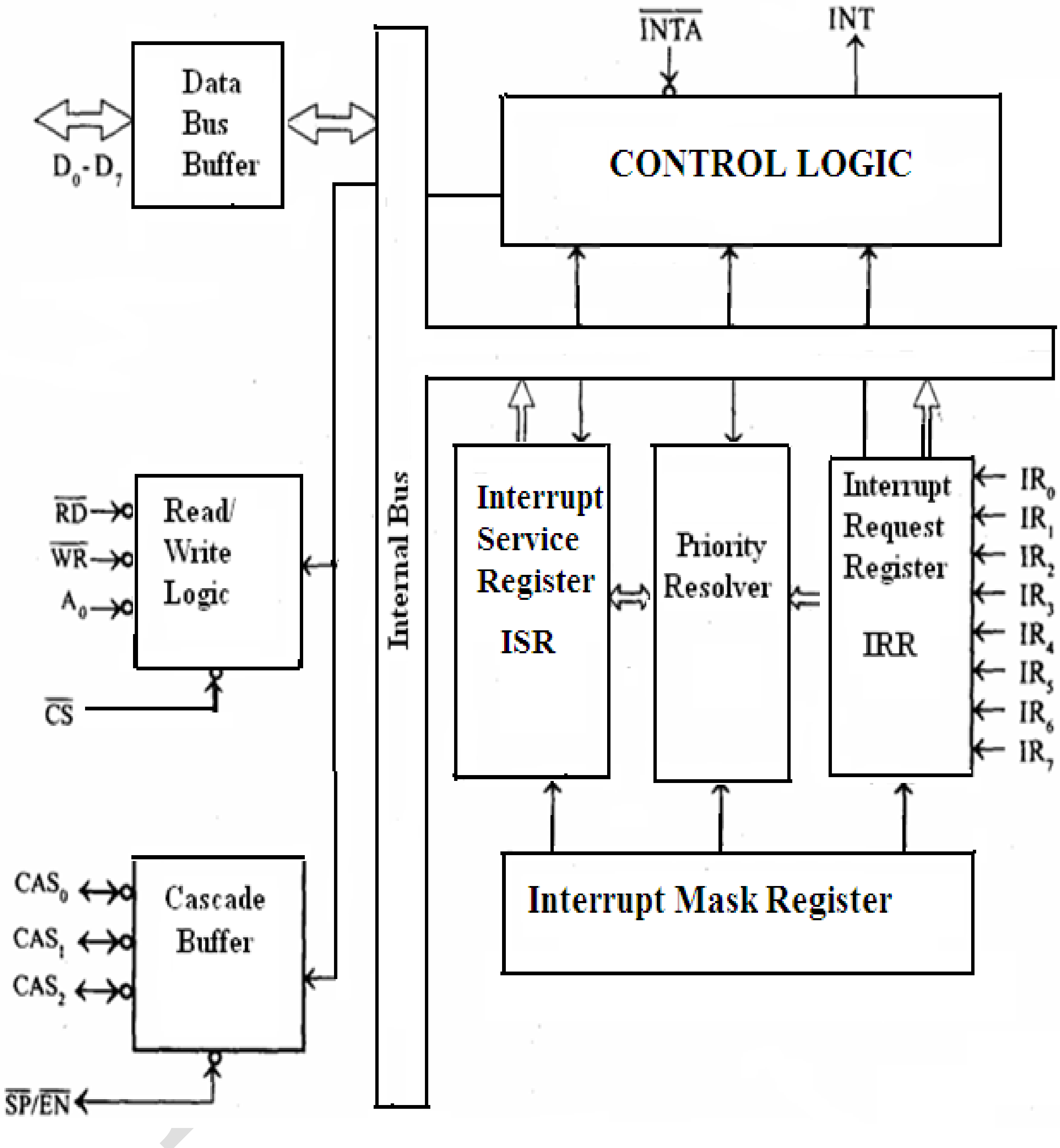

Figure 6: Block Diagram of 8259

WORKING OF 8259

The 8259 accepts interrupt requests from any one of the 8 I/O lines (IR_0 - IR_7). Then it ascertains the priority of the interrupt lines. Then it ascertains the priority of the interrupt lines. Suppose, the received interrupt has higher priority than currently serviced, it interrupts the microprocessor and after receiving the interrupt acknowledgement from microprocessor. It provides a 3 byte CALL instruction. The sequence of steps that occur when an interrupt request line of 8259 goes high is as follows.

- The 8259 accepts the requests on IR_0 - IR_7 in IRR. Then it checks the contents of IMR whether that request is masked or not.
- The 8259, then checks ISR to know the interrupt levels that are being currently serviced. After this 8259 sends a high INT to 8085 processor. Normally, it is the job of the priority resolver to check the contents of IRR, IMR and ISR and decide whether to activate INT output of 8259 or not.
- Now 8085 processor responds by suspending the program flow at the end of the current instruction and makes low.
- On receiving, 8259 sends code for CALL to the microprocessor on D_{7-0} bus.
- This code for CALL in IR register of 8259 causes the 8085 to issue two more signals. When goes low the second time, 8259 places LSB of ISS address on the data bus. When goes low the third time, 8259 places the MSB of ISS address ont he data bus.
- Now, the microprocessor branches to the ISS after saving the contents of program counter on the stack top.
- After finishing the ISS, the control returns to the main program by popping the top of stack to PC.

Programming 8259

The 8259 requires two types of command words namely, Initialization Command Words (ICW) and Operational Command Words (OCW). The 8259 can be initialized with four ICWs, the first two are essential and the other two are optional based on the modes being used. These words must be issued in a sequence. Once the 8259 is initialized, the 8259 can operate in various modes by using three different OCWs.

PROGRAMMABLE INTERVAL TIMER - 8253/54

Introduction

It is always possible to generate accurate time delays using the microprocessor system by using software loop programs. But that will waste the precious time of CPU. Hence INTEL introduced the chips 8253/8254 which is a hardware solution for the problem of generating accurate time delays. These chips can be used for applications such as a real-time clock, event counter, a digit alone shot, a square wave generator and also as a complex wave form generator.

Salient Features

- 8254 is an upgraded version of 8253 and they are pin-compatible.
- 8254 can operate with higher clock frequency ranging from DC to 8 MHz and 10 MHz, whereas the 8253 can operate with clock frequency from DC to 2 MHz.
- 8254 includes a status read-back command that can latch the count and the status of the counters. This command is not available in 8253.
- 8253 uses N-MOS technology where as 8254 uses H-MOS technology.
- The chips are packaged in 24 pin DIP and requires a single +5V DC power supply.
- Three identical 16 bit counters that can operate independently in any of the six modes are available. The counters are down counters.
- These chips are compatible with all INTEL and most of the other microprocessors.
- To operate a counter, a 16 bit count is loaded in its register and on command beings to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can be used to interrupt the microprocessor.
- The counters can be programmed for either binary or BCD count.
- The read-back command of 8254 allows the user to check the count value and current status of the counter.

PIN CONFIGURATION OF 8253/8354:

The chips 8253/54 is packaged in a 24 pin DIP and require a single +5V power supply. The pin diagram is shown in Fig. The description of each pin is given below.

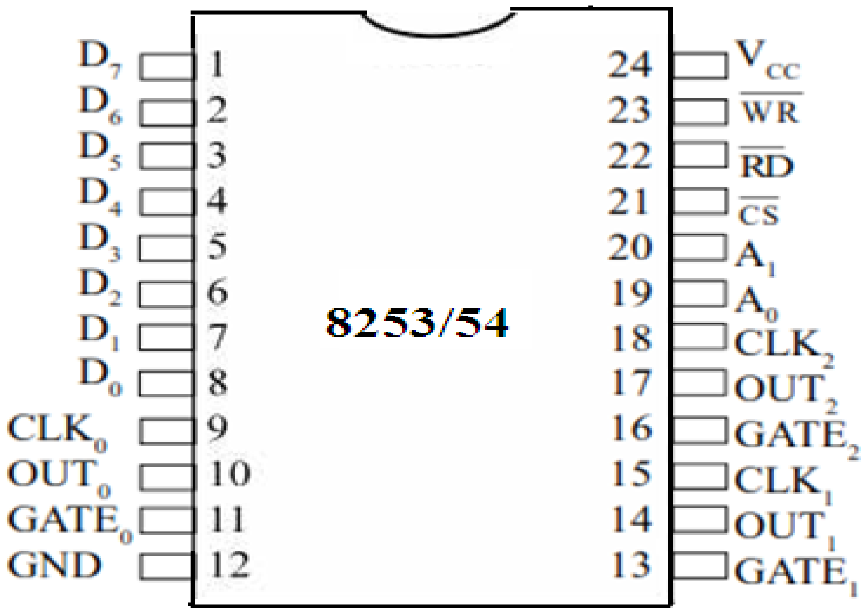

Figure 11: Pin Diagram of 8253/54

Pin symbol	Function
$D_0 - D_7$	8 bit Data bus for transfer of data
CLK N	Input pulses for counter clocks (CLK 0, CLK 1, CLK 2)
$GATE_n$	Input pulses for counter gates (GATE 0, GATE 1, GATE 2)
OUT N	Outputs of the counters (OUT 0, OUT 1, OUT 2)
	Active low. Reads the contents of the counter
	Active low. Data can be written to counters by CPU when the pin is low.
	Active low pin. Selects the chip
A_0 - A_1	Counter select address lines used to select one of the three counters
V_{CC}	+5 volts
GND	Ground

Table 3:Pin function

BLOCK DIAGRAM OF 8253/8254

The block diagram of the Programmable Interval Timer is shown in Fig. The block diagram includes three counters - Counter 0, Counter 1 and Counter 2, a data bus buffer, read/write control logic and a control word register. Each counter has two input signals CLOCK and GATE and one OUTPUT signal-out.

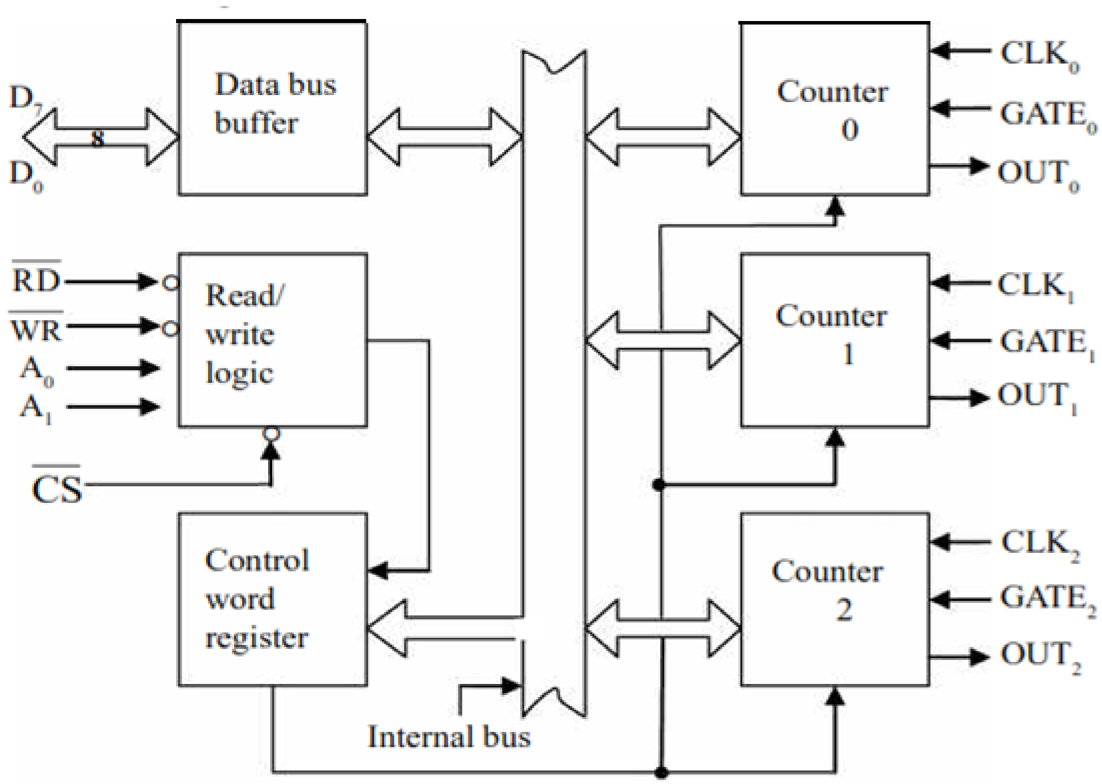

Figure 12: Block Diagram of 8253/8254

Data Bus Buffer

This tri-state bidirectional 8 bit buffer is used to interface the 8253 to the system bus. Data is transmitted or received by the buffer upon execution of INPUT or OUTPUT CPU instructions. The data bus buffer has three basic functions. They are

i. Programming the MODES of the 8253.

ii. Loading the count registers and

iii. Reading the count values.

Read/Write Logic

The read/write logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by so that no operation can occur to change the function unless the device is selected by the system logic.

RD : A low on this pin informs the 8253 that the CPU is inputting data in the form of counters value.

WR : It is an active low pin. A low on this pin informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A_0,A_1: These two lines are address lines used to select one of the three counters and the control word register as shown in the table for mode selection.

CS(Chip Select): It is an active low pin. A low on this input enables 8253. No read or write will occur unless the device is selected. The input has no effect on the actual operation of the counters.

A_0	A_1				Function
X	X	X	X	1	Tri state
0	0	0	1	0	Read from counter 0
0	1	0	1	0	Read from counter 1
1	0	0	1	0	Read from counter 2
1	1	0	1	0	No operation - Tri state
0	0	1	0	0	Write to counter 0
0	1	1	0	0	Write to counter 1
1	0	1	0	0	Write to counter 2
1	1	1	0	0	Write to counter word
X	X	1	1	0	Tri state

Table 4: Selection and function of 8253/54 Counters

CONTROL WORD REGISTER:

- This register is selected when A_0, A_1 are at logic 1. It then accepts the information from the data bus buffer and stores it in a register.
- The information stored in this register controls the operation MODE of each counter, selection of binary or BCD counting and the loading of each count register.

- The control word register can only be written to into, but no read operation is possible.

Counter 0, Counter 1, Counter 2

- These three functional blocks are identical in operation. Each counter consists of a single 16 bit, pre-settable DOWN counter.
- The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the control word register.
- The counters are totally independent. The counter can be read by a simple READ operation for event count applications.

Operational Description

- The complete functional operation of 8253 is programmed by the system software.
- A set of control words must be sent out by the CPU to initialize each counter of 8253/8254 with the desired MODE.
- Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to perform.

The actual counting operation of each counter is totally independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the micro computer system have been eliminated.

PROGRAMMING 8253/54

Each counter of 8253/54 is individually programmed by writing a control word into control word register. The control word register is shown in Figure below. The different bits of this 8 bit register are either set or reset for the operation of the counters.

The various options are given below.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

Table 5: Control Word Format

- Counter selection is done by the D_6, D_7 bits.

SC_1	SC_0	Remarks
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal for 8253. Read back
		command for 8254

Table 6: Counter selection is done by the D_6, D_7 bits

- The bits D_4, D_5 decides the counter READ/LOAD operations as shown below.

RL_1	RL_0	Remarks
0	0	Counter latching operation
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only
1	1	Read/Load LSB first then MSB

Table 7: D_4, D_5 decides the counter READ/LOAD operations

- The bits D_1, D_2 and D_3 decide the mode operation 8253/54 can be configured in six modes. This mode selection is done by these bits as shown below.

M_2	M_1	M_0	Remarks
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

Table 8: mode operation 8253/54

- The D_0 bit decides whether the counter is a 16 bit binary counter or a BCD counter.
- When $D_0 = 0$ it acts as a 16 bit binary counter.
- $D_0 = 1$ it acts as a binary coded decimal counter (BCD)

While using 8253/54 we must write the control word to initialize the counter to be used. For every counter we use, the control word must be written and select the counter and set it up. 8253/54 can operate in six different modes. The modes of operation are explained below.

Mode 0 (Interrupt on Terminal Count)

- The output of the counter will be initially low after the mode set operation.
- After the count is loaded into the selected counter register the output will remain low and the counter will count.
- When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded.

Mode 1 (Programmable one shot)

- In this mode, the out signal is initially high. When the GATE is triggered, the OUT goes low, and when count reaches 0, the OUT goes high again.
- Thus a one shot signal is generated due to the signal on the GATE.

Mode 2 (Rate Generator)

- It is a divide by N counter. In this mode, a pulse is generated that is equal to the clock period at a given interval controlled by the count that is loaded.
- When the count is loaded, the OUT signal stays high until the count reaches 1, at this point the OUT signal goes low for one clock period.
- Afterwards, the count is reloaded automatically and the cycle repeats, generating a continuous string of pulses.

Mode 3 (Square-wave Generator)

- In this mode, when the count is loaded, the OUT signal is high. The count is then determined by two with each clock cycle.
- When the count reach 0 the OUT signal goes low and the count is reloaded automatically. As this is repeated continuously a square wave is generated on the OUT signal.
- The period of the square wave is controlled by the count value.

Mode 4 (Software Triggered Strobe)

- In this mode, the OUT signal is initially high and goes low for one clock period when the count reaches 0.
- S_0, one strobe pulse (low) is generated for each count. The count must be reloaded for more strobe signals.

Mode 5 (Hardware - Triggered Strobe)

- This mode is similar to mode 4, except the strobe is hardware triggered with a signal on the GATE signal. The OUT signal is initially high.
- When the GATE signal goes from low to high, the count starts and when it reaches 0, the OUT signal goes low for one clock period.

Read-Back Command

- The read-back command in the 8254 allows the user to read the count and the status of the counters (This command is not available in 8253).
- When the read-back command is selected in the control word (SC_1 SC_0 - 11) each of the counters specified is latched and then the count and/ or the status may be read for each counter latched.

The command is written in the control register and the count of the specified counter(s) can be latched if COUNT (bit D_5) is 0. A counter or a combination of counters is specified by making the respective CNT bits (D_1, D_2 and D_3) high. The read-back command format is shown below.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{\text{COUNT}}$	$\overline{\text{STATUS}}$	CNT2	CNT1	CNT0	0

Table 9: Read back command format

- D_0 = 0 (Reserved for future expansion)
- CNT0, CNT1, CNT2 are counter select bits.

The STATUS of the counters can be read if D_4 bit (STATUS) of Read-back command is 0. The Read-back command eliminates the need of writing separate counter latch commands for different counters.